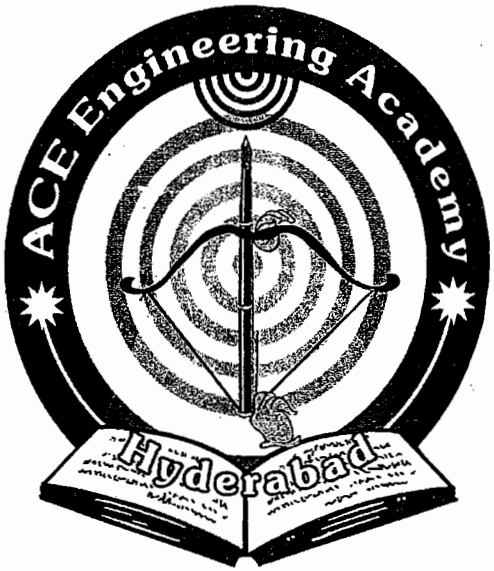


GATE - SYLLABUS

Electronic Devices: Energy bands in silicon, intrinsic and extrinsic silicon. Carrier transport in silicon: diffusion current, drift current, mobility, and resistivity. Generation and recombination of carriers. p-n junction diode, Zener diode, tunnel diode, BJT, JFET, MOS capacitor, MOSFET, LED, p-I-n and avalanche photo diode, Basics of LASERs. Device technology: integrated circuits fabrication process, oxidation, diffusion, ion implantation, photolithography, n-tub, p-tub and twintub CMOS process.

ELECTRONIC DEVICES

CONTENTS

For

GATE, DRDO, PSUs & IES

Managing Director

Y.V. Gopala Krishna Murthy

CHAPTER – I SEMICONDUCTOR THOERY

(Electrons and holes in semiconductors, carriers statistics, mechanics of current flow in semiconductors, hall effect)

ATOMIC STRUCTURE

- Every element has characteristic atoms.
- Atoms of different elements contain electrons, which are completely identical.
- Atoms of every element have a positively charged nucleus. Almost entire mass of the atom is concentrated in the nucleus.
- The atom is composed of a positively charged nucleus surrounded by negatively charged electrons and the neutrons carry no charge.
- Mass of an atom is very small, mass of a carbon atom, 12_C, is only 1.992678×10^{-26} kg.
- Protons and neutrons are the constituents of a nucleus. The no. of protons (called the atomic number) and the no. of neutrons represented by the symbol Z and N respectively.
- The total no. of neutrons and protons in a nucleus is called its mass number A (=Z+N).
- Atom as a whole is electrically neutral and therefore contains equal amount of positive and negative charges.
- The radius of the electron has been estimated as 10^{-15}m, and that of an atom as 10^{-10}m.
- The electron surrounding the nucleus in an atom occupies different orbits.
- The mass of the electron is negligible compared to that of protons and neutrons, the mass of the atom depends mostly on the number of protons and neutrons in the nucleus.
- The basic unit of charge is the charge of the electron. The MKS unit of charge is the coulomb. The electron has a charge of 1.602×10^{-19} coulomb and that of the electron rest mass is 9.109×10^{-31} kg.
- The electron has a charge of 1.602×10^{-19} coulomb, it follows that a current of 1 ampere corresponds to the motion of $1 / (1.602 \times 10^{-19}) = 6.24 \times 10^{13}$ electrons past any cross section of a path in 1 second.
- The valence orbit can hold no more than eight electrons. When the valence orbit has eight electrons, it is saturated.
- If an atom loses an electron, it becomes a positive ion with a net charge of +1. If it gains an extra electron, it becomes a negative ion with a charge of –1.
- "Ionization potential" is the energy required to remove an electron from the outer orbit of an atom. The size of the atom decreases considerably, as more and more electrons are removed from the outer orbit.
- The work done by the system, when the extra electron is attracted form infinity to the outer orbit of the neutral atom, is known as the "electron affinity" and correspondingly an increase in the size of the atom.
- The tendency of an atom to attract electrons to itself during the formation of bonds with other atoms is measured by the "electro negativity" of that atom.
- The magnitude of energy released, when two atoms come together from a large distance of separation to the equilibrium distance, is called the "bond energy".

- "Ionic bonding" forms between two oppositely – charged ions, which are produced by the transfer of electrons from one atom to another.
- Sharing of electrons between neighboring atoms results in a "covalent bond", which is directional.
- Covalent bonding occurs by the sharing of electrons between neighboring atoms. This is in contrast to the transfer of electrons from one atom to another in the ionic bonding.
- The force on a unit positive charge at any point in an electric field is, by definition, the electric field intensity ε at that point.
- The force on a positive charge **q** in an electric field of intensity ε is given by **qε**, the resulting force being in the direction of the electric field. Thus, $\mathbf{f_q = q\varepsilon}$
  where $\mathbf{f_q}$ is in newtons, **q** is in coulombs and ε is in volts per meter.

  The magnitude of the charge on the electron is **e**, the force on an electron in the field is **f = -eε** .The minus sign denotes that the force is in the direction opposite to the field.
- A unit of work or energy, called the electron volt (eV), is defined as follows:
  $1\ eV = 1.602 \times 10^{-19}$ J
- The name electron volt arises from the fact, if an electron falls through a potential of one volt, its kinetic energy will increase by the decrease in potential energy, or by
  $eV = (1.602 \times 10^{-19} c)(1V) = 1.602 \times 10^{-19}$ J = 1eV
- The force of attraction between the nucleus and the electron is $\mathbf{e^2/(4\pi\varepsilon_0 r^2)}$ in newtons,
  where e = electron charge in coulombs
  r = separation between the two particles in meters
  ε_0 = permittivity of free space.
- The potential energy of the electron at a distance **r** from the nucleus is $\mathbf{-e^2/(4\pi\varepsilon_0 r)}$, and its kinetic energy is $\mathbf{(1/2)mv^2}$.
- The total energy of the electron in Joules is $\mathbf{w = -e^2 / (8\pi\varepsilon_0 r)}$ [Rutherford atomic model]
- This expression shows that the energy of the electron becomes smaller (i.e., more negative) as it approaches closer to the nucleus.
- The minimum energy required for the electron to escape from the metal at absolute zero of temperature is called the "work function E_w".
- The total energy of electron in stationary states in Joules and in electron volts is given by [Bohr atomic model].

$$W_n = \frac{(-me^4)}{(8\varepsilon_0^2 h^2 n^2)} \text{ Joules}$$

$$W_n = \frac{(-me^3)}{(8\varepsilon_0^2 h^2 n^2)} \text{ eV} = \frac{-13.6}{n^2} \text{ eV}$$

Where m = electronic mass in kilograms
h = Planck's constant in Joules - seconds
n=orbit number

- It should be noted that the energy is negative and therefore, the energy of an electron in its orbit increases as 'n' increases.

- To remove an electron from the first orbit (n = 1) of the hydrogen atom to outside of the atom, that is to ionize the atom, the energy required is 13.6 eV. This is known as the "ionization energy" or the "ionization potential" of the atom.
- The energy associated with an electron in **n**th orbit of the hydrogen atom is $\mathbf{E_n = (13.6)/n^2}$ eV. Thus the energies $E_1, E_2, E_3, \ldots$ of the first, second, third, ... ∞ orbits are respectively -13.6, -3.4, -1.51, ... 0 eV. The energy required to raise the atom from the ground state (n = 1) to the first excited state is (13.6 – 3.4) = 10.2 eV. The energy required to raise it to the second excited state is (13.6 – 1.51) = 12.09 eV and so on. It is clear that 10.2 eV, 12.09 eV are excitation potentials while 13.6 eV is the ionization potential of the hydrogen atom.
- The lowest energy level E_1 is called the normal or the ground state of the atom and the higher energy levels $E_2, E_3, E_4, \ldots$ are called the excited states.
- The emitted radiation by its wavelength λ in angstroms, when electron transition from one state to the other state is

$$\lambda = \frac{12{,}400}{E_2 - E_1}$$

and this energy is emitted in the form of a proton of light.

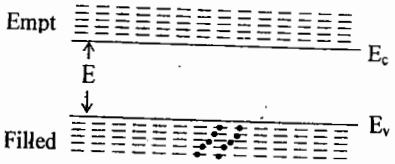
- **Atomic concentration** $\mathbf{n = (A_o d) / A}$ atoms/cm^2
  A = atomic weight d = density A_o = Avogadro number

For Germanium	**For Silicon**
A = 72.6	A = 28
d = 5.32 g/cm^3	d = 2.33 g/cm^3
$A_o = 6.023 \times 10^{23}$ molecules/ mole	$A_o = 6.023 \times 10^{23}$ molecules/ mole
Then, $n = 4.4 \times 10^{22}$ atoms/cm^3	Then, $n = 5 \times 10^{22}$ atoms/cm^3

$\mathbf{n_{Si} > n_{Ge}}$, because atomic number of silicon is less than atomic number of Germanium.

Energy Band Theory of Crystals

- The inter – atomic spacing is gradually decreases, there will be a gradual increase in the interaction between the neighboring atoms. Due to this interaction, the atomic wave functions overlap, and the crystal becomes an electronic system which should obey the Pauli's exclusion principle.
- An energy gap exists between the two energy bands. This energy gap is called as forbidden energy gap $\mathbf{E_G}$, as no electrons can occupy states in this gap.
- The band below energy gap $\mathbf{E_G}$ is called Valence band. The band above the energy gap $\mathbf{E_G}$ is called conduction band.
- The upper band, called the conduction band, consists of infinitely large number of closely spaced energy states. The lower band, called the valence band, consists of closely spaced completely filled energy states and only two electrons are allowed in each energy state according to Pauli's exclusion principle as shown in fig.



- The electrons in the valence band would not move under the action of applied voltage or field because of completely filled energy states. Therefore, the valence electrons do not conduct.
- The electrons in the upper (or conduction band) can, however, gain momentum and move since there are closely spaced empty available states in the band.
- At equilibrium spacing, the lowest conduction band energy is E_c and highest valence band energy is E_v.
- The gap between the top of the valence band and bottom of the conduction band is called 'energy band gap'(Energy gap).It may be large, small or zero, depending upon the material.
- The bottom of the conduction band corresponds to zero electron velocity or kinetic energy and simply gives us the potential energy at that point in space.
- For holes, the top of the valence band corresponds to zero kinetic energy.

Insulators, Semiconductors and Metals

- A very poor conductor of electricity is called an insulator; an excellent conductor is a metal;and a substance whose conductivity lies between these extremes is semiconductor.

Insulator:-

- For a diamond (Carbon) crystal the region containing no quantum states is several electron volts high. ($E_G \approx 6eV$). This large forbidden band separates the filled valence region from the vacant conduction band, and therefore no electrical conduction is possible. Insulator is a negative temperature coefficient of resistance.
- The energy gap is so large that electrons cannot be easily excited from the valence band to the conduction band by any external stimuli (Electrical, thermal or optical).

Metal: - This refers to a situation, where the conduction and valence bands are overlapping. This is the case of a metal where $E_G = 0$. This situation makes a large number of electrons available for electrical conduction and, therefore the resistance of such materials is low or the conductivity is high.

Semiconductor: - A substance for which the width of the forbidden energy region is relatively small (~ 1eV) is called a semiconductor.

- The most important practical semiconductor materials are germanium and silicon, which have values of E_G of 0.785 and 1.21 eV, respectively, at 0°K.
- Energies of this magnitude normally cannot be acquired from an applied field.
- Hence the valence band remains full, the conduction band empty, and these materials are insulators at very low temperatures (≈ 0°K).
- However, the conductivity increases with temperature as we explain below, and for this reason these substances are known as "intrinsic semiconductors".
- As the temperature is increased, some of these valence electrons acquire thermal energy greater than E_G and hence move into the conduction band.
- These thermally excited electrons at T > 0K, partially occupy some states in the conduction band which have come from the valence band leaving equal number of holes there.
- The phrase "holes in a semiconductor" refers to the empty energy levels in an otherwise filled valence band.

- The importance of the hole is that it may serve as a carrier of electricity, comparable in effectiveness with the free electron.
- As the temperature of a semiconductor is reduced to zero, all valence electrons remain in valence band.
- If a certain impurity atoms are introduced into the crystal, these result in allowable energy states which lie in the forbidden energy gap. These impurity levels also contribute to the conduction.
- A semiconductor material where this conduction mechanism predominates is called an "extrinsic (impurity) semi conductor".
- The energy gap E_G for silicon decreases with temperature at the rate of 3.60×10^{-4} eV/°K. Hence, for silicon,

$$E_G(T) = 1.21 - 3.60 \times 10^{-4}\, T$$

and at room temperature (300°K), $E_G = 1.1$ eV.

- Similarly for germanium,

$$E_G(T) = 0.785 - 2.23 \times 10^{-4}\, T$$

and at room temperature, $E_G = 0.72$ eV

- The fundamental difference between a metal and a semiconductor is that the former is unipolar (conducts current by means of charges (electrons) of one sign only); where as a semiconductor is bipolar (contains two charge carrying "particles" of opposite sign(electrons and holes)).

Current Density:- If N electrons are contained in a length **L** of conductor (fig) and if it takes an electron a time **T** sec to travel a distance of **L** meter in the conductor, the total number of electrons passing through any cross section of wire in unit time is **N/T**.

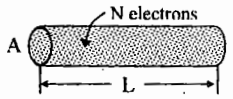


Fig.

Thus the total charge per second passing any point, which by definition is the current in amperes, is **I = Nq / T** .....(eq.1) Where $q = 1.602 \times 10^{-19}$ C

By definition, the current density, denoted by the symbol J, is the current per unit area of the conducting medium, i.e, assuming a uniform current distribution **J = I /A** .....(eq.2)

Where **J** is in amperes per meter square, and **A** is the cross – section area (in meters) of the conductor. This becomes, by eq.1 **J = Nq / TA** .....(eq.3)

But it has been pointed out that the average, or drift, speed **v** m/sec of the electrons, is

V = L/T i.e., **T = L/ v**

Then, the eq.3 becomes **J = Nqv / LA** .....(eq.4)

From above fig. it is evident that **LA** is simply the volume containing the **N** electrons, and so **(N/LA)** is the electron concentration **n** (in electrons per cubic meter). Thus

n = N/LA And eq.4 reduces to **J = n qv = ρ V**

Where **ρ = nq** is the charge density, in coulombs per cubic meter, and **v** is in meters per second.

Mobility and Conductivity:

- If a constant electric field ε (Volts per meter) is applied to a substance, the electrons would be accelerated and a finite value of drift velocity v is attained.
- This drift velocity v is in the direction opposite to that of the electric field, and its magnitude is proportional to ε. Thus $\boxed{v = \mu\varepsilon}$ ε = electric field

  Where μ (m^2 / V – s) is called the mobility of the electrons.
- The directed flow of electrons with a drift velocity v constitutes a current.
- If the concentration of free electrons is **n** (electrons per cubic meter), the current density **J** (amperes per square meter) is

$\boxed{J = nqv = nq\mu\varepsilon = \sigma\varepsilon}$ Where q = electron charge = 1.602×10^{-19} C and

$\boxed{v=\mu\varepsilon}$ $\boxed{\sigma = nq\mu}$ is the conductivity of the substance in (ohm – meter)$^{-1}$

- The conductivity is proportional to the concentration n of free electrons.

Mobilities of Electrons and Holes in Silicon and Germanium

Species	Mobility at room temperature, m^2 / V-sec	
	Silicon	Germanium
Electrons	0.14	0.39
Holes	0.05	0.19

- By observing the above table, the electron mobility is about three times the hole mobility.
- For a good conductor, **n** is very large (~ 10^{28} electrons / m^3); for an insulator, **n** is very small (~ 10^7); and for a semiconductor, **n** lies between these two values.
- In a certain temperature range, the electrical conductivity of a semiconductor increases with increase in temperature. This is because the carrier concentration increases substantially, but the mobility of carriers decreases with increase in temperature.
- The parameter μ varies as T^{-m} over a temperature range of 100 to 400°K. For silicon, m = 2.5 (2.7) for electrons (holes), and for germanium, m = 1.66(2.33) for electrons(holes). The mobility is also found to be a function of electric field intensity ε and remains constant only if $\varepsilon < 10^3$ V/cm in **n** – type silicon. For $10^3 < \varepsilon < 10^4$ V/cm, μ_n varies approximately as $\varepsilon^{-1/2}$. For higher fields, μ_n is inversely proportional to ε and the carrier speed approaches the constant value of 10^7 cm/s.

Electrons and Holes in an Intrinsic Semiconductor

- Germanium (Ge) and Silicon (Si) are the two most important semiconductors used in electronic devices.
- The crystal structure of these materials consists of a regular repetition in three dimensions of a unit cell having the form of a tetrahedron.
- Each atom in a Ge(Si) crystal contributes four valence electrons, so that the atom is tetravalent.

- Each of the valence electrons of a Ge(Si) atom is shared by one of its four nearest neighboring atoms.
- The bonding between this electron pair is a covalent bond.
- At a very low temperature (say 0°K), semiconductor behaves as an insulator, since no free carriers of electricity are available.
- At room temperature, some of the covalent bonds will be broken because of the thermal energy supplied to the crystal, and conduction is made possible.
- The energy E_G required to break such a covalent bond is about 0.72 eV for germanium and 1.1 eV for silicon at room temperature.
- Hole in a lattice is designed as vacancy created by removal of electron from covalent bond.
- The absence of the electron in the covalent bond (incomplete) is called a hole.
- The importance of the hole is that it may serve as a carrier of electricity comparable in effectiveness to the free electron.
- The motion of the hole in one direction actually means the transport of a negative charge an equal distance in the opposite direction.
- So far as the flow of electric current is concerned, the hole behaves like a positive charge equal in magnitude to the electronic charge. We can consider that the holes are physical entities whose movement constitutes a flow of current.
- In a pure (intrinsic) semiconductor the number of holes in a valence band is equal to the number of free electrons in the conduction band.
- Thermal agitation continues to produce new hole – electron pairs, whereas other hole – electron pairs disappear as a result of recombination.
- Two types of carrier flow exist in an intrinsic semiconductor. First, there is the flow of free electrons through larger orbits (Conduction band). Second, there is the flow of holes through smaller orbits (Valence Band).

Conductivity of a Semiconductor

- With each hole – electron pair created, two charge – carrying particles are formed.
- One is negative (free e^-) of mobility μ_n, and the other is positive (hole) of mobility μ_p.
- The current density **J** is given by

$$\boxed{J = (n\mu_n + p\mu_p)q\varepsilon = \sigma\varepsilon}$$

Where n = magnitude of free – electron (negative) concentration
p = magnitude of hole(positive) concentration
σ = conductivit; ε = electric field and q = electron charge
Hence

$$\boxed{\sigma = (n\mu_n + p\mu_p)q}$$

- The resistivity ρ is inversely proportional to the conductivity and is given by

$$\boxed{\rho = 1/\sigma = 1/(n\mu_n + p\mu_p)q}$$

- For a pure (called intrinsic) semiconductor considered here,
  - $n = p = n_i$ Where n_i is the intrinsic concentration
- In pure germanium at room temperature there is about one hole – electron pair for every 2×10^9 germanium atoms.
- With increasing temperature, the density of hole – electron pair increases and correspondingly, the conductivity increases.

$n_i^2 = A_0 T^3 e^{-E_{GO}/KT}$

- The intrinsic concentration n_i varies with temperature in accordance with the relationship.
  Where A_0 = material constant
  T = temperature in degree Kelvin
  E_{GO} = energy gap at 0°K in eV
  K = Boltzmann constant in eV/°K
- The conductivity of germanium (Silicon) is increase approximately 6(8) percent per degree increase in temperature.
- The resistivity (reciprocal of conductivity) of a semi conductor decreases exponentially where in metals the resistivity increases almost linearly.
- Semiconductor has a negative temperature coefficient of resistance where as that of a metal is positive and of much smaller magnitude.
- For most metals the resistance increases about 0.4 percent / °C increase in temperature.
- The constants E_{GO}, μ_n, μ_p and many other important physical quantities for Germanium and

Properties of Germanium and Silicon

Property	Ge	Si
Atomic number.....	32	14
Atomic weight	72.6	28.1
Density, g/cm^3.....	5.32	2.33
Dielectric constant (relative).....	16	12
Atoms / cm^2	4.4×10^{22}	5.0×10^{22}
E_{GO}, eV, at 0°K	0.785	1.21
E_G, eV, at 300°K.....	0.72	1.1
n_i at 300°K, cm^{-3}.....	2.5×10^{13}	1.5×10^{10}
Intrinsic resistivity at 300°K, Ω - cm	45	230,000
μ_n, cm^2/V-s at 300°K	3800	1300
μ_p, cm^2/V-s at 300°K	1800	500
D_n, cm^2/s = $\mu_n V_T$	99	34
D_p, cm^2/s = $\mu_p V_T$	47	13

Silicon are given in Table. Note that germanium has of the order of 10^{22} atoms/cm^3, whereas at room temperature (300°K), $n_i = 10^{13}$/cm^3. Hence only 1 atom in about 10^9 contributes a free electron (and also a hole) to the crystal because of broken covalent bonds. For silicon this ratio is even smaller, about 1 atom in 10^{12}

Carrier Concentration in an Intrinsic Semiconductor:

- The free electrons occupy successive quantum states of increasing kinetic energy.
- The energy corresponding to the highest filled level at 0°K is called the 'Fermi energy E_F'.
- At 0°K, the free electrons occupy all the levels up to the Fermi level, leaving all those above it empty.
- At temperature above 0°K, due to thermal excitation, there is a finite probability of some of the electrons from below the Fermi level moving to levels above E_F.
- This probability is given by the Fermi – Dirac statistics.
- The probability of occupation f(E) of an energy level E by an electron is given by

$$f(E) = \frac{1}{(1 + \exp(E - E_F)/KT)}$$

- The Fermi level can be defined as that level which has a 50% probability of occupation by an electron at any temperature.

Case (1): At T = 0°K

$f(E) = 1/(1 + e^{\infty}) = 0$ when $E > E_F$

$f(E) = 1/(1 + e^{-\infty}) = 1$ when $E < E_F$

- Intrinsic semiconductor will acts as insulator for 0°K
- Case(2) : At T = 300°K

$f(E) = 0$ when $E >> E_f$

$f(E) = 1$ when $E << E_f$

As temperature increases conduction increases in intrinsic semiconductor.

$$KT = 0.026 \text{ eV} = 26 \text{ meV}$$

For $E >> E_c$, $E - E_F >> KT$ and equation reduces to $f(E) = e^{-(E - E_c)/kT_f}$

E_c = lowest energy level in the conduction band

The electron concentration n is proportional to f(E).

$n \propto e^{-(E_c - E_f)/kT}$

$$n = N_c e^{-(E_c - E_f)/kT}$$

where

$N_c = 2[(2\pi m_n kT)/h^2)]^{3/2} (1.602 \times 10^{-19})^{3/2} = 2[(2\pi m_n \bar{k}T)/h^2]^{3/2}$

$\bar{k} = ke$

k is given in electron volts per degree kelvin (eV / °K)

$\bar{k}$ is expressed in Joules per degree kelvin (J / °K)

m_n = effective mass of electron

m = Rest mass of electron

N_c = Conduction constant = $4.82 \times 10^{15} (m_n/m)^{3/2} . T^{3/2}$ per cm^3

- Similarly hole concentration is

$$p = N_v e^{-(E_f - E_V)/kT}$$

Where N_v = valence concentration = $4.82 \times 10^{15} (m_p/m)^{3/2} T^{3/2}$ per cm^3.
m_p = effective mass of hole
m = rest mass of electron, because at rest hole does not exist.

- The above equations (for **n** and **p**) apply to both intrinsic and extrinsic or impure semiconductors.
- When an electron in a periodic potential is accelerated relative to the lattice in an electric field or magnetic field then the mass of that electron is called "effective mass".
- n_i < 2.5×10^{13} carriers / cm^3 → Ge (at room temperature)
  1.5×10^{10} carriers / cm^3 → Si (at room temperature)
- Where n_i is no. of carriers (or) no. of covalent bonds that are broken for the given temperature.

The Fermi Level in an Intrinsic Semiconductor

- In the case of intrinsic material **n = p**

$$N_c e^{-(E_c - E_f)/kT} = N_v e^{-(E_f - E_v)/kT}$$

Hence

$$E_f = \frac{(E_c + E_v)}{2} - \frac{kT}{2} \ln \frac{N_c}{N_v}$$

- If the effective masses of a hole and a free electron are the same(i.e.,$N_c = N_v$),then the above equation reduces to

$$E_f = \frac{(E_c + E_v)}{2}$$

- Hence the Fermi level lies in the center of the forbidden energy band.

The Intrinsic Concentration

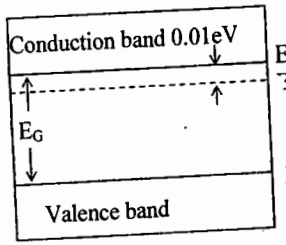
- Using above equations, the product of electron – hole concentrations

$$np = N_c N_v e^{-(E_c - E_v)/kT} = N_c N_v e^{-E_G/kT}$$

- Note that this product is independent of the Fermi level, but does depend upon the temperature and the energy gap $E_G = E_c - E_v$. The above equation is valid for either and extrinsic or intrinsic material.
- Hence, for intrinsic material $n = p = n_i$, we have the important relationship (called the mass – action law) $np = n_i^2$
- Note that, regardless of the individual magnitudes of **n** and **p**, the product is always a constant at a fixed temperature.
- At room temperature, the current in an intrinsic semiconductor is due to both e⁻ and holes.
- In an intrinsic semiconductor the mobility of electrons in the conduction band is greater than the mobility of holes in the valence band.

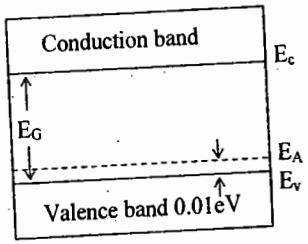
Donor and Acceptor Impurities

- If, to a pure germanium, a small amount of impurity is added in the form of a substance with five valence electrons, four of the five valence electrons will occupy covalent bonds, and the fifth will be nominally unbound and will be available as a carrier of current.
- The energy required to detach this fifth electron from the atom is of the order of only 0.01 eV for **Ge** and 0.05 eV for **Si**.
- Suitable pentavalent impurities are phosphorous, arsenic, antimony and bismuth (PAAB). Such impurities donate excess (negative) electron carriers and are therefore referred to as "donor, or n – type" impurities.
- When donor impurities are added to a semiconductor, allowable discrete energy levels are introduced a very small distance below the conduction band, as shown in below fig. and therefore at room temperature almost all of the "fifth" electrons of the donor material are raised into the conduction band.
- If intrinsic semiconductor material is "doped" with n – type impurities, not only does the number of electrons increase, but the number of holes decreases below that which would be available in the intrinsic semiconductor.
- The reason for the decrease in the number of holes is that the larger number of electrons present increases the rate of recombination of electrons with holes.
- If a trivalent impurity (Boron, Aluminium, Gallium and Indium(BAGI)) is added to an intrinsic semiconductor, only three of the covalent bonds can be filled and the vacancy that exists in the fourth bond constitutes a hole.
- Such impurities make available positive carriers because they create holes which can accept electrons.
- These impurities are consequently known as "acceptor, or p – type" impurities.
- When acceptor, or p – type impurities are added to the intrinsic semiconductor, they produce an allowable discrete energy levels which is just above the valence band.
- A very small amount of energy is required for an e⁻ to leave the valence band and occupy the acceptor energy level E_v, it follows that the holes generated in the valence band by these electrons constitute the largest number of carriers in the semiconductor material.
- The doping of intrinsic semiconductor not only increases the conductivity, but also serves to produce a conductor in which the electric carriers are either predominantly holes or e⁻s.
- In an n – type semiconductor, the electrons are called the majority carriers, and the holes are called the minority carriers.
- In a p – type material, the holes are the majority carriers, and the electrons are the minority carriers.
- Intrinsic, p – type and n – type semiconductors are electrically neutral, i.e., the total negative charge is equal to that of total positive charge.



E_D = Donor energy level

Fig: Energy band diagram of n – type semiconductor



E_A =Acceptor energy level

Fig: Energy band diagram of p – type semiconductor.

- The minority-carrier concentration injected into one end of a semiconductor bar decreases exponentially with distance into the specimen (as a result of diffusion and recombination)
- Semiconductor, p^+ - type: A p-type semiconductor in which the excess mobile hole concentration is very large (i.e. more doping).
- Semiconductor, n^+ - type: An n-type semiconductor in which the excess conduction electron concentration is very large (i.e. more doping).

Charge Densities in a Semiconductor:

$np = n_i^2$

gives the relationship between the electron **n** and the hole **p** concentrations.

- Let N_D equal the concentration of donor atoms, these are practically all ionized, N_D positive charges per cubic meter are contributed by the donor ions.
- Hence the total positive charge density is $N_D + p$
- Similarly, if N_A is the concentration of acceptor ions, these contribute N_A negative charges per cubic meter.
- The total negative charge density is $N_A + n$.
- Since the semiconductor is electrically neutral, the magnitude of the positive charge density must equal that of the negative concentration, or

$$N_D + p = N_A + n \qquad \text{---- (1)}$$

- Consider an n – type material having $N_A = 0$. Since the number of electrons is much greater than the number of holes in an n – type semiconductor ($n >> p$) then equation (1) reduces to

$$n \simeq N_D \quad \text{or} \quad n_n \simeq N_D$$

- In an n – type material the free – electron concentration n_n is approximately equal to the density of donor atoms.
- The concentration p_n of holes in the n – type semiconductor is obtained from

$$n_n p_n = n_i^2$$

Thus, $\boxed{p_n = n_i^2 / N_D}$

- Similarly, for a p – type semiconductor

$$\boxed{n_p p_p = n_i^2 \quad ; \quad p_p \simeq N_A \quad n_p = n_i^2/N_A}$$

- According to the law of mass action, the product of the number of electrons in the conduction band and the number of holes in the valence band must be constant.

Fermi level in a semiconductor having impurities

- The electrical characteristics of a semiconductor material depend on the concentration of free electrons and holes.
- In the case of no impurities (an intrinsic semiconductor), E_F lies in the middle of the energy gap, indicating equal concentrations of free electrons and holes in conduction band and valence band respectively.
- n – type semiconductor

In n – type semiconductor

$$n \approx N_D$$

$$n = N_D = N_c e^{-(E_C - E_F)/kT}$$

Solving for E_F,

$$E_C - E_F = kT \ln (N_C / N_D)$$

where N_D = Donor concentration

= atomic concentration × Doping rate

For example Germanium, doping rate = $1 : 10^8$

$$N_D = (4.4 \times 10^{22}) \times 1/10^8$$

Case:1 Doping increases, N_D increases and then $N_D > N_C$

$$E_C - E_F = kT \ln(N_C / N_D) < 0$$

$$E_C < E_F$$

- As doping concentration increases Fermi level moves towards conduction band from center of the forbidden gap and hence conduction increases.

Case(2) : If temperature increases, N_C increases and then $N_C > N_D$

$$E_C - E_F > 0$$

$$E_C > E_F$$

- As temperature increases Fermi level moves towards the center of the forbidden energy gap and hence conduction decreases in extrinsic semiconductor.

- For p – type semiconductor:

$$p \approx N_A$$
$$= N_A = N_V e^{-(E_F - E_V)/kT}$$
$$E_F - E_V = kT \ln(N_V / N_A)$$

N_A = acceptor concentration

Case(1): Doping increases, N_A increases
and then, $N_A > N_V$
$E_F - E_V = kT \ln(N_V / N_A) < 0$
$E_F - E_V < 0$
$E_F < E_V$

- As doping increases Fermi level moves towards valence band from center of forbidden gap and hence conduction increases.

Case(2): If temperature increases, N_V increases
and then $N_V > N_A$
$E_F - E_V > 0$
$E_F > E_V$

- Fermi level moves towards the center of the forbidden energy gap and hence conduction decreases in extrinsic semiconductor.

	n – type	p – type	conduction
Doping increases	E_F goes up	E_F goes down	Increases
Temperature Increases	E_F goes down	E_F goes up	Decreases

TEMPERATURE EFFECT ON EXTRINSIC SEMICONDUCTOR

At very low temperature range the conductivity is an exponential function of temperature. The electron excited from the donor level to the conduction band (or the holes created by excitation to the acceptor level) becomes available in increasing numbers with increasing temperature. So, the conductivity increases as the temperature increases upto certain level that depends on doping concentration.

Increasing temperature, the density of carriers will increases results in decreasing mean free path of the conduction electrons or holes. So, the conduction decreases with increasing temperature.

At extraordinary high temperatures extrinsic will behave as intrinsic semiconductor.

Drift and Diffusion Currents:

- The conductivity associated with the conduction electrons could be written in the form

$\sigma_n = n \mu_n q$ where μ_n = mobility of the electrons
q = electron charge
Similarly for hole conduction
$\sigma_p = p \mu_p q$ where μ_p = mobility of holes

- The current density associated with the drift of the electrons due to the applied field would be given by

$$J_n = n \mu_n q\varepsilon$$

Similarly, $J_p = p \mu_p q\varepsilon$

- However, an electron current may flow in a semiconductor even in the absence of an electric field, i.e., if there exists a gradient of the electron density.
- Consequently, one deals in semiconductors frequently with two kinds of current: a drift current (due to the electric field) and diffusion current (due to a gradient of the carrier concentration).
- These concepts apply, of course, to electrons as well as to holes.
- The diffusion current density for electrons is $J_n = q D_n \frac{dn}{dx}$
- D_n = Diffusion constant of the electrons in m^2/sec.
- Similarly, diffusion current density for holes is

$J_p = -q D_p \frac{dp}{dx}$ D_p = diffusion constant of the holes in m^2/sec.

- The hole current in any point x may be written as the sum of two contributions, one from the field and one from the diffusion process:

$$J_p = p \mu_p q\varepsilon - q \frac{D_p}{dx} dp$$

- Similarly, the total electron current density:

$$J_n = n \mu_n q\varepsilon + q \frac{D_n}{dx} dn$$

- There exists an important relationship between the diffusion coefficient and the mobility of the carriers, which is known as the Einstein relation:

For holes $D_p = (kT/q) \mu_p$
For electrons $D_n = (kT/q) \mu_n$

- Hence, the diffusion constant is proportional to the mobility

$$\frac{D_p}{\mu_p} = \frac{Dn}{\mu_n} = V_T$$

Where $V_T = kT/q = T/11,600$ where V_T = volt equivalent of temperature
At room temperature (300°K), μ = 39 D =26 mV at room temperature

$\boxed{k = 1.602 \times 10^{-19} k}$

Carrier Life Time

- Thermal agitation continues to produce new hole – electron pairs while other hole electron pairs disappear as a result of recombination.
- On an average, a hole (an electron) will exist for $\tau_p(\tau_n)$ seconds before recombination. This time is called the "mean life time" of the hole and electron, respectively.
- Carrier life times range from nanoseconds to hundreds of microseconds.
- $\tau_p(\tau_n)$ is the time it takes the injected concentration to fall to 1/e of its initial value.

- Recombination is effected not only by volume impurities, but also by surface imperfections in the crystal.
- Gold is extensively used as a recombination agent.
- Thus the device designer can obtain desired carrier life times by introducing gold into silicon under controlled conditions.

The continuity equation

- It is also called law of conservation of energy in semiconductor.
- The continuity equation, or the equation of conservation of charge for holes is
  $dp/dt = -(p - p_0)/\tau_p + D_p(d^2p/dx^2) - \mu_p.d(p\varepsilon)/dx$
- If τ_p is the average carrier lifetime of holes, the (p/τ_p) equals the holes per second lost by recombination per unit volume.
- $p_0(n_o)$ is the equilibrium concentration of holes(electrons). Hole (electron) concentration $p(n)$ is a function of both time **t** and distance **x**.
- Similarly the continuity equation for electrons is **p** replaced by **n** in the above equation.
- The diffusion length for holes is given by $L_p = \sqrt{(D_p \tau_p)}$
- Similarly for electrons $L_n = \sqrt{(D_n \tau_n)}$
- From continuity equation we can say that it is the time taken by the carriers for the concentration to become $1/\epsilon$ times of initial concentration.

The Hall Effect

- If a specimen (metal or semiconductor) carrying a current **I** is placed in a transverse magnetic field **B**, an electric field ε is induced in the direction perpendicular to both **I** and **B**. This phenomenon, known as the "Hall Effect".
- The Hall voltage $V_H = \varepsilon d = Bvd = (BJd)/\rho = (BI)/(\rho w)$

Where d = distance between two surfaces; w = width of the specimen
J = current density; v = drift velocity
ρ = charge density.

$\rho = nq$ or pq q = charge of electron

- The Hall coefficient R_H is defined by

$$R_H = 1/\rho = (V_H w)/(BI)$$

$$R_H = 1/\rho = 1/(N_D q) = 1/(N_A q)$$

- If conduction is due primarily to charges of one sign, the conductivity σ is related to the mobility μ by $\sigma = \rho\mu$

- If the conductivity is measured together with the Hall coefficient R_H, the mobility can be determined from $\mu = \sigma R_H$
- The Hall coefficient R_H of an intrinsic semiconductor is negative under all conditions.
- In an extrinsic semiconductor, the Hall coefficient R_H increases with increase of temperature.

Applications of Hall Effect:

- The Hall effect is used to determine the following
  (i) type of semiconductor
  (ii) carrier concentration
  (iii) mobility and
  (iv) magnetic flux density
- Why carbon is not used as semiconductor?
  The carbon (C), Silicon(Si) and Germanium (Ge) all have the same number of valence electrons (4), but their resistivities widely differ.
  The energy required to take out an electron from these atoms (i.e., ionization energy E_G) will be least for Ge, followed by Si and highest for C.
  Hence, number of free electrons for conduction in Ge and Si are significant but negligibly small for C.

	Temperature range	Energy gap at 0°K
Carbon	-65°C to 225°C	> 5 eV
Silicon	-65°C to 175°C	1.21 eV
Germanium	-65°C to 75°C	0.78 eV

OBJECTIVES - 1

01. Energy required to break a covalent in semiconductor is
  (a) always equal to 1.6 e V
  (b) greater in Ge than in Si
  (c) equal to the width of the forbidden energy gap
  (d) is the same in Ge as in Si
02. The diffusion length of a carrier depends on
  (a) the shape of the semiconductor
  (b) the life time of the carriers alone
  (c) the mobility and life time of the carriers
  (d) the mobility of the carriers alone.
03. Pure semiconductors are poor conductor because
  (a) they have no valence electrons
  (b) all valence electrons are in e⁻-pairs
  (c) they have a number of holes
  (d) there are fewer e⁻s than protons
04. At room temperature, the current in an intrinsic semiconductor is due to
  (a) holes (b) electrons
  (c) ions (d) holes and electrons

05. At room temperature intrinsic carrier concentration is higher in germanium than in silicon because
(a) carrier mobilities are higher Ge than in Si
(b) energy gap in Ge is smaller than that in Si
(c) Atomic no. of Ge is larger than in Si
(d)Atomic weight of Ge is larger than in Si

06. Current flow in a semiconductor depends on the phenomenon of
(a) drift (b) diffusion
(c) recombination (d)all of the above

07. The effect of doping in intrinsic semiconductor is to
(a) move the Fermi level away from the centre of the forbidden band
(b) move the Fermi level towards the centre of the forbidden band
(c) change the crystal structure of the semiconductor
(d) keep the Fermi level at the middle of the forbidden band

08. n-type semiconductors
(a) are negatively charged
(b) are produced when indium is added as an impurity to germanium
(c) are produced when phosphorus is added as an impurity to silicon
(d) none of the above

09. If a sample of germanium and a sample of silicon have the same impurity density and are kept at room temperature
(a) both will have equal value of resistivity
(b) both will have equal negative resistivity
(c) resistivity of germanium will be higher than that of silicon
(d) resistivity of silicon will be higher than that of germanium

10.Semiconductor A has a higher band gap than semiconductor B. If both A and B have the same dimensions, the same number of electrons at a given temperature and the same electron and hole mobilities, then
(a) A has the same number of holes as B
(b) A has larger number of holes than B
(c) A has lesser number of holes than B
(d) any of the above statements at a, b or c, could be true

11. If the temperature of an extrinsic semiconductor is increased so that the intrinsic carrier concentration is double, then
(a) the majority carrier density doubles
(b) the minority carrier density doubles
(c) the minority carrier density becomes times the original value
(d) both majority and minority carrier densities doubles

12. In a semiconductor, rate of diffusion of charge carriers
(a) depends on the concentration gradient and the mobility
(b) depends on the concentration gradient alone.
(c) depends on the mobility alone
(d) is independent of concentration gradient and the mobility

13. Donor impurity atom in a semiconductor result in new
(a) wide energy band
(b) narrow energy band
(c) discrete energy level just below conduction level
(d) discrete energy level just above valence level.

14. Mobility of electron in a semiconductor
(a) decreases as the temperature increases
(b) increases as the temperature increases
(c) has no effect on conductivity
(d) is independent of temperature

15. If donor concentration N_D equals acceptor concentration N_A resulting semiconductor is
(a) n-type (b) p-type (c) intrinsic
(d) may be p or n type depending on temperature

16. A semiconductor is damaged by a strong current, because
(a) Excess of electrons
(b) Decrease in electrons
(c) Lack of free electrons (d) None

17. When a semiconductor bar is heated at one end, a voltage across the bar is developed. If the heated end is positive, the semiconductor is
(a) p-type (b) n-type
(c) intrinsic (d) highly degenerate

18. Hall effect device can be used to
(a) Add two signals
(b) Multiply two signals
(c) Subtract one signal from another
(d) Divide one signal by another on an instantaneous basis

19. A semiconductor is uniformly doped with N_A acceptors and N_D donors. Let the free electron and hole concentrations be n and p respectively. Assume that the semiconductor is at thermal equilibrium and that 100% ionization has taken place. Then which of the following is true?
(a) $N_A + N_D = p + n$
(b) $N_A - N_D = n - p$
(c) $N_A N_D = pn$
(d) $N_D - N_A = n - p$

20. Which of the following statements is true?
(a) Silicon doped with either phosphorous only or boron only is p-type semiconductor
(b) Silicon doped with either phosphorous only or boron only is n-type semiconductor.
(c) Silicon doped with phosphorous is n-type semiconductor.
(d) Silicon doped with boron is n-type semiconductor.

ANSWERS :

1. C	**2.C**	**3.B**	**4.D**	**5.B**	**6.D**	**7.A**	**8.C**	**9.D**	**10.B**
11. D	**12.A**	**13.C**	**14.A**	**15.C**	**16.A**	**17.B**	**18.B**	**19.D**	**20. C**

OBJECTIVES - 2

01. Diffusion of impurities in a semiconductor is carried out in a furnace through which a steady stream of impurity atoms is passed during the entire diffusion process. What would be the type of profile of the impurity atoms inside the semiconductor?
(A) Linear
(B) Gaussian
(C) complementary error function
(D) exponential

02. Excess carriers are generated in a sample of N-type semiconductors by shining light at one end. The current flow in the sample will be made up of
(a) diffusion flow of carriers
(b) drift flow of carriers
(c) both diffusion and drift flow of carriers
(d) neither diffusion nor drift flow of carriers

03. A semiconductor is irradiated with light such that carries are uniformly generated throughout its volume. The semiconductor is n-type with $N_D = 10^{19}$ per cm3. If the access electron concentration in the steady state is $\Delta n = 10^{15}$ per cm3 and if $Zp = 10\mu$ sec (minority carrier life time) the generation rate due to irradiation
(a) is 10^{20} e-h pairs/cm^3/sec
(b) is 10^{24} e-h pairs/cm^3/sec
(c) is 10^{10} e-h pairs/cm^3/sec
(d) cannot be determined as the given data is insufficient

04. A long specimen of p-type semiconductor material
(a) is positively charged
(b) is electrically neutral
(c) has an electrical field directed along its length
(d) acts as a dipole

05. If an intrinsic semiconductor is doped with a very small amount of boron, then in the extrinsic semiconductor set formed, the number of electrons and holes will
(a) decrease
(b) increase and decrease respectively
(c) increase
(d) decrease and increase respectively

06. Under high electric field, in a semiconductor with increasing electric field
(a) The mobility of charge carriers decreases.
(b) The mobility of charge carriers increases.
(c) The velocity of the charge carriers saturates.
(d) The velocity of charge carriers increases.

07. A silicon sample is uniformly doped with 10^{16} phosphorous atoms/cm^3 and 2×10^{16} boron atom /cm^3. If all the dopants are fully ionized, the material is
(a) n-type with carrier concentration of $10^{16}/cm^3$
(b) p-type with carrier concentration of $10^{16}/cm^3$
(c) p-type with carrier concentration of $2x\ 10^{16}/cm^3$
(d) n-type with carrier concentration of $2x1\ 0^{16}/cm^3$

08. The probability that an electron in a metal occupies the fermi level at any temperature (>0^0K).
(a) 0 (b) 1 (c) 0.5 (d) 0.1

09. Pure Si is experimentally determined to exhibit a carrier (electron or hole) density of $1.48X\ 10^{10}$electrons (holes) cm^3 at 300 ^{0}k.If the electron mobility and hole mobility is 1300cm^2/Vs and 500 cm^2/Vs,the resistivity of an intrinsic Si specimen at 300^{0}k is..
(a) $2.35X\ 10^5\ \Omega$m (b) $1.18X\ 10^5\ \Omega$m
(c) $2.35X\ 10^5\ \Omega$cm
(d) cannot be determined

10. Mobility μ varies as T^m over a temperature range of 100 to 400^0 k. For silicon, m = ... for holes.
(a) 2.5 (b) 2.7
(c) 1.66 (d) 2.33

11. In an n-type silicon, mobility is found to be a function of electric field intensity. If electric field intensity (E) applied is in the range:
R_1 : 500 V/cm - 883 V/cm &
R_2: 500 V/cm - 8830 V/cm, then for the above ranges R_1 & R_2, the mobility varies as
(a) constant, constant
(b) $\varepsilon^{-1/2}$, ε^{-1}
(c) ε^{-1}, $\varepsilon^{-1/2}$
(d) constant, $\varepsilon^{-1/2}$

12. Match List-I (Material) with List-II (Energy Level) and select the correct answer using the code given below the lists:

List-I
A. p-type semiconductor at 0^0 K
B Intrinsic semiconductors at 0^0 K
C. n-type semiconductor at room temperature
D. p-type semiconductor at room temperature

List-II
1. Donor energy level is closed to the conduction band
2. Acceptor energy level is closed to the valence band
3. Fermi-level is very closed to valence band
4. Fermi-level is half-way between the valence band and the conduction band

Codes:

	A	B	C	D
(a)	1	2	3	4
(b)	3	4	1	2
(c)	1	4	3	2
(d)	3	2	1	4

13. Match List-I (Current) with List-II (Variation) and select the correct answer using the code given below the lists:

List-I	List-II
A. Hole diffusion current	1. n.E
B. Electron drift current	2. p.E
C. Hole drift current	3. dp/dx
D. Electron diffusion current	4. dn/dx

Codes:

	A	B	C	D
(a)	2.	1	3	4
(b)	3	4	2	1
(c)	2	4	3	1
(d)	3	1	2	4

14. Match List -I (Device) with List -II (Application) and select the correct answer using the code given below the lists:

List-I	List-II
A. Hall element	1. Power control
B. Varactor diode	2.microwave mirror
C. SCR	3. Tuning element in tank circuit
D. Schottky	4. Sensor

Codes:

	A	B	C	D
(a)	2	3	1	4
(b)	4	1	3	2
(c)	2	1	3	4
(d)	4	3	1	2

15. The free electron density in a conductor is $(1/1.6) \times 10^{22}$ cm^{-3}. The electron mobility is 10 cm^2/ Vs. What is the value of its resistivity?
(a) $10^{-4}\ \Omega$m
(b) $1.6X\ 10^{-2}\ \Omega$m
(c) $10^{-4}\ \Omega$cm
(d) 10^4 mho.cm^{-1}

16 Match List-I (Type of conductor) with List-II (Position of Fermi Level) and select the correct answer using the code given below the lists:

List-I

A. n-type semiconductor
B. P-type semiconductor
C. Intrinsic semiconductor
D. Degenerate n-type semiconductor

List – II

1. Middle of band gap
2. Above conduction band
3. Near but below conduction band
4. Near but above valence band

Codes:

	A	B	C	D
(a)	1	2	3	4
(b)	3	4	1	2
(c)	1	4	3	2
(d)	3	2	1	4

17. Match List-I with List-II and select the correct answer using the code given below the lists:

List-I

A. Drift current
B. Einstein's equation
C. Diffusion current
D. Continuity equation

List- II

1. Law of conservation of charge
2. Electric field
3. Thermal Voltage
4. Concerntration Gradient

Codes:

	A	B	C	D
(a)	2	1	4	3
(b)	4	3	2	1
(c)	4	1	2	3
(d)	2	3	4	1

18. If in intrinsic semiconductor Germanium at 300K (27^0C) the charge concentration and mobilities of free electrons and holes are 2.5 x 10^{13} per CC, 3.8 x 10^3 cm^2 / v-sec and 1.8 x 10^3 cm^3/v- see respectively, then its resistivity at 300K is

(a) 230 x 10^3 cm (b) 100 cm
(c) 44.6 cm (d) 22.3 cm

19. A small concentration of minority carries is injected into a homogeneous semiconductor crystal at one point. An electricfield of 10 V/cm is applied across the crystal and this moves the minority carriers a distance of 1 cm in 20 μ sec. The mobility (in cm^2/voltsec) of the minority carriers is

(a) 1,000 (b) 2,000
(c) 5,000 (d) 500,000

20. In a Hall effect experiment, a p type semiconductor sample with hole concentration p_1 is used. The Measured value of the hall voltage is V_{H1}. If the p – type sample is now replaced by another p – type sample with hole concentration p_2 where $p_2 = 2p_1$, what is the new Hall voltage V_{H2}?

(a) $2V_{H1}$ (b) $4 V_{H1}$
(c) $(1/2) V_{H1}$ (d) $(1/4) V_{H1}$

KEYS :

01. c	02.a	03.a	04.b	05.d	06.a
07.b	08.b	09.c	10.b	11.d	12.b
13.d	14.d	15.c	16.b	17.b	18.c
19.c	20.c				

PREVIOUS IES QUESTIONS:

01. A Hall effect transducer can be used to measure
(a) displacement, temperature and magnetic flux.
(b) displacement, position and velocity
(c) position, magnetic flux and pressure
(d) displacement, position and magnetic flux.

02. The Ohm's law for conduction in metals is
(a) $J = \sigma E$ (b) $J = E/\sigma$
(c) $J \propto \sigma E$ (d) $J \propto E/\sigma$

03. The unit of a thermal resistance of a semiconductor device is
(a) Ohms (b) Ohms/^{0}C
(c) ^{0}C/Ohm (d) ^{0}C/Watt

04. For n-type semiconductor with $n = N_D$ and $p = n_i^2/N_D$, the hole concentration will fall below the intrinsic value because some of the holes
(a) drop back to acceptor impurity states
(b) drop to donor impurity states
(c) virtually leave the crystal
(d) recombine with the electrons

05. Match **List-I with List-II** and select the correct answer using the codes given below the lists:

List-I

A. Drift current
B. Einstein's equation
C. Diffusion current
D. Continuity equation

List-II

1. Law of conservation of charge
2. Electric field
3. Thermal voltage
4. Concentration gradient

Codes:

	A	B	C	D
(a)	2	1	4	3
(b)	4	3	2	1
(c)	4	1	2	3
(d)	2	3	4	1

06. Consider the following statements:
If an electric field is applied to an n-type semiconductor bar, the electrons and holes move in opposite directions due to their opposite charges. The net current is
1. due to both electrons and holes with electrons as majority carriers.
2. the sum of electron and hole currents.
3. the difference between electron and hole current.

Which of these statements is/are correct?
(a) 1 alone (b) 1 and 2
(c) 2 alone (d) 2 alone

07. **Assertion(A):** Hall crystal can be used as a multiplier of two signals.
Reason(R): Hall voltage is proportional to the current or voltages applied in perpendicular directions across the Hall crystal.
(a) Both A and R are true and R is the correct explanation of A.
(b) Both A and R are true but R is NOT the correct explanation of A.
(c) A is true but R is false.
(d) A is false but R is true.

08. As the Fermi energy of silver is 8.8×10^{-19} joule, the velocity of the fastest electron in silver at 0^0K (Given: Rest mass of electron = 9.1 x 10^{-31} kg) is
(a) 3.33 x 10^5 m/s (b) 1.39 x 10^6 m/s
(c) 4.40 x 10^7 m/s (d) 3 x 10^8 m/s

09. Electron mobility and life – time in a semiconductor at room temperature are respectively 0.36 m^2/ (Vs) and 340μs. The diffusion length is
(a) 3.13 mm (b) 1.77 mm
(c) 3.55 mm (d) 3.13 cm

10. Which of the following statements relate to the Hall effect?
1. A potential difference is developed across a current - carrying metal strip when the strip is placed in a transverse magnetic field.
2. The Hall effect is very weak in metals but is large in semiconductors.
3. The Hall effect is very weak in semiconductors but is large in metals.
4. It is applied in the measurement of the magnetic field intensity.
(a) 1, 2 and 3 (b) 2 and 4
(c) 1, 3 and 4 (d) 1, 2 and 4

11. **Assertion (A):** The intrinsic Fermi level of a semiconductor does not lie exactly at the middle of the energy band gap.
Reason(R): The densities of the available states in valance and conduction bands of a semiconductor are equal.
(a) Both A and R are true and R is the correct explanation of A.
(b) Both A and R are true but R is NOT the correct explanation of A.
(c) A is true but R is false.
(d) A is false but R is true.

12. The conductivity of a semiconductor crystal due to any current is NOT proportional to
(a) mobility of the carrier
(b) effective density of states in the conduction band.
(c) electronic charge
(d) surface states in the semiconductor

13. The unit of mobility is
(a) $m^2V^{-1}s^{-1}$ (b) $mV^{-1}s^{-1}$
(c) Vsm^{-1} (d) Vms^{-1}

14. In an extrinsic semiconductor, the Hall coefficient R_H
(a) increases with increase of temperature
(b) decreases with increase of temperature
(c) is independent of the change of temperature.
(d) changes with the change of magnetic field.

15. Consider a semiconductor bar having square cross – section. Assume that holes drift in the positive x -direction and magnetic field is applied perpendicular to the direction in which holes drift. The sample will show
(a) a negative resistance in positive y-direction.
(b) a positive voltage in positive y-direction.
(c) a negative voltage in positive y-direction.
(d) a magnetic field in positive y-direction.

16. Consider the following statements for an n-type semiconductor:
1. Donor level ionization decreases with temperature.
2. Donor level ionization increases with temperature.
3. Donor level ionization is independent of temperature.
4. Donor level ionization increases as E_D (donor energy level) moves towards the conduction band at a given temperature.
Which of these statements is/are correct?
(a) 1 only (b) 2 only
(c) 2 and 4 (d) 3 only

17. Consider the following statements for an n-type semiconductor:
1. E_F lies below E_D at a room temperature(T).
2. E_F lies above E_D as $T \to 0$
3. $E_F = E_D$ at some intermediate temperature.
4. E_F is invariant with temperature.
Where E_F is Fermi energy and E_D is donor level energy. Which of these statement(s) is/are correct?
(a) 1 and 2 (b) 2 and 3
(c) 4 only (d) 1, 2 and 3

18. Assume $n_i = 1.45 \times 10^{10}/cm^3$ for silicon. In an n-type silicon sample, the donor concentrated at 300 K is $5 \times 10^{14}/cm^3$ and corresponds to 1 impurity atom for 10^8 silicon atoms. The electron and hole concentrations in the sample will be
(a) $n = 5 \times 10^{14}/cm^3$ $p = 4.2 \times 10^5/cm^3$
(b) $n < 5 \times 10^{14}/cm^3$ $p > 4.2 \times 10^5/cm^3$
(c) $n > 5 \times 10^{14}/cm^3$ $p < 4.2 \times 10^5/cm^3$
(d) $n < 5 \times 10^{14}/cm^3$ $p < 4.2 \times 10^5/cm^3$

19. A semiconductor specimen of breadth d, width w and carrying current I is placed in a magnetic field B to develop Hall voltage v_H in a direction perpendicular to I and B. V_H is NOT proportional to (a) B (b) I
(c) 1/w (d) 1/d

20. **Assertion (A):** The conductivity of a semiconductor is decided by the level of its doping and is almost independent of its band gap value irrespective of temperature.
Reason(R): The carrier concentration due to doping is independent of temperature, if it is not too low.
(a) Both A and R are true and R is the correct explanation of A.
(b) Both A and R are true but R is NOT the correct explanation of A.
(c) A is true but R is false.
(d) A is false but R is true.

21. Consider the following statements
The intrinsic concentration of semiconductor
1. depends on doping
2. increases exponentially with decrease of band gap of the semiconductor
3. increases non-linearly with increase of temperature
4. increases linearly with increase of temperature
Which of the statements given above are correct?
(a) 1, 2 and 3 (b) 1 and 3
(c) 2 and 3 (d) 2 and 4

22. Consider the following statements:
During an electron transition the energy gap in an indirect energy gap material like silicon
1. the momentum of the electron changes
2. the direction of motion of the electron changes
3. the potential energy of the electron changes
4. the kinetic energy of the electron changes
Which of the statements given above are correct?
(a) 1, 2 and 3 (b) 2, 3 and 4
(c) 1, 3 and 4 (d) 1, 2 and 4

23. **Assertion (A):** The concentration measured by Hall effect does not have much significance if the semiconductor is non-homogeneously doped.
Reason (R): The current density is uniform throughout the thickness of the semiconductor.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

24. The mobility of electrons in a semiconductor is defined as the
(a) Diffusion velocity per unit electric field
(b) Diffusion velocity per unit magnetic field
(c) Drift velocity per unit magnetic field
(d) Drift velocity per unit electric filed

25. The free electron density in a conductor is (1/1.6) x (10^{22} cm^{-3} The electron mobility is 10 cm^2/Vs. What is the value of its resistivity?
(a) $10^{-4}\Omega m$ (b) $1.6 \times 10^{-2}\Omega m$
(c) $10^{-4}\Omega cm$ (a) 10^{1}mho cm^{-1}

26. The intrinsic concentration in a semiconductor at 300K is 10^{13} cm^{-3}. When it is doped with donor type impurities, the majority carrier concentration becomes 10^{17} cm^{-3}. What is the value of its minority carrier density?
(a) $0.999 \times 10^{17} cm^{-3}$ (b) $10^{17} cm^{-3}$
(c) $10^{4} cm^{-3}$ (d) 10^{9} cm^{-3}

27. Two pure specimen of a semiconductor material are taken. One is doped with 10^{18} cm^{-3} number of donors and the other is doped with 10^{16} cm^{-3} number of acceptors. The minority carrier density in the first specimen is 10^{7} cm^{-3}. What is the minority carrier density in the other specimen/
(a) 10^{16} cm^{-3} (b) 10^{27} cm^{-3}
(c) 10^{18} cm^{-3} (d) 10^{9} cm^{-3}

28. Match **List-I** (Type of Conductor) with **List-II** (Position of Fermi Level) and select the correct answer using the codes given below the lists:

List-I
A. n-type semiconductor
B. p-type semiconductor
C. intrinsic semiconductor
D. Degenerate n-type semiconductor

List-II
1. Middle of band gap
2. Above conduction band
3. Near but below conduction band
4. Near but above valence band

Codes:

	A	B	C	D
(a)	1	2	3	4
(b)	3	4	1	2
(c)	1	4	3	2
(d)	3	2	1	4

29. Match List – I (Material) with List – II (Carrier Concentration / m^3) an select the correct answer using the codes given below the lists:

List – I
A. Intrinsic semiconductor
B. Insulator
C. Extrinsic semiconductor
D. Conductor

List – II
1. 10^{28}
2. 10^{22}
3. 10^{18}
4. 10^{14}

Codes:

	A	B	C	D
(a)	3	4	2	1
(b)	2	1	3	4
(c)	3	1	2	4
(d)	2	4	3	1

30. Mobility is defined as
(a) diffusion velocity per unit field
(b) drift velocity per unit field
(c) displacement per unit field
(d) number of free electrons/ number of bound electrons

31. **Assertion (A):** An n – type semiconductor behaves as an intrinsic semiconductor at very high temperatures.
Reason (R): The breaking of the covalent bonds becomes a significant phenomenon at high temperatures.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

32. **Assertion (A):** Electron mobility in metals decreases with increasing temperature.
Reason (R): In metals electron concentration in high.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

33. Which of the following can be determined by using a Hall crystal?
1. Concentration of holes in a p – type semiconductor
2. Concentration of electrons in an n – type semiconductor
3. Temperature of the set – up with any type of semiconductor
4. Diffusion constant and life – time of minority carriers of any type of semiconductor
Select the correct answer using the code given below:
(a) Only 1 and 2
(b) 1, 2 and 4
(c) Only 3 and 4
(d) Only 2 and 4

34. Match List – I (Current) with List – II (Variation) and select the correct answer using the code given below the lists:

List – I	List - II
A. Hole diffusion current	1. n. E
B. Electron drift current	2. p. E
C. Hole drift current	3. – dp/dx
D. Electron diffusion current	4. dn/dx

Codes:

	A	B	C	D
(a)	2	1	3	4
(b)	3	4	2	1
(c)	2	4	3	1
(d)	3	1	2	4

35. Match List – I (Material) with List – II (Energy Level) and select the correct answer using the code given below the lists

List – I
A. p – type semiconductor at 0 K temperature
B. Intrinsic semiconductor at 0 K temperature
C. n – type semiconductor at room temperature
D. p – type semiconductor at room temperature

List – II

1. Donor energy level is close to the conduction band
2. Acceptor energy level is close to the valence band
3. Fermi – level is half – way between the valence band and the conduction band:

Codes:

	A	B	C	D
(a)	1	2	3	4
(b)	3	4	1	2
(c)	1	4	3	2
(d)	3	2	1	4

36. An intrinsic semiconductor (intrinsic electron density = 10^{16} m^{-3}) is doped with donors to a level of 10^{22} m^{-3}. What is the hole density assuming all donors to be ionized?

(a) 10^{7} m^{-3} (b) 10^{8} m^{-3}

(c) 10^{10} m^{-3} (d) 10^{6} m^{-3}

37. Why does the mobility o electrons in a semiconductor decrease with increasing donor density?

(a) Doping increases the effective mass of electrons
(b) Doping increases the relaxation time of electrons
(c) Electrons are trapped by the donors
(d) More holes are generated so that the effective mobility decreases

38. Match List – I (Item) with List – II (Position) and select the correct answer using the code given below the lists:

List – I

A. Donor energy band
B. Fermi level of p – type semiconductor at room
C. Acceptor energy band
D. Fermi level in intrinsic semi – conductor

List – II

1. At the middle of the forbidden energy gap
2. Close to the conduction band temperature
3. Very close to the valence band
4. Close to the valance band

Codes:

	A	B	C	D
(a)	4	3	2	1
(b)	2	1	4	3
(c)	4	1	2	3
(d)	2	3	4	1

39. The electron and hole concentrations, n and p respectively obey the relation $np = n_i^2$ where n_i is the intrinsic carrier density. This expression is valid for which of the following?

(a) For all semiconductors under any condition
(b) For direct band gap semiconductor only
(c) For non – degenerate semiconductor under thermal equilibrium condition
(d) For degenerate semiconductors having excess electrons and holes

40. An intrinsic semiconductor is doped lightly with p – type impurity. It is found that the conductivity actually decreases till a certain doping level is reached. Why does this occur?

(a) The mobility of holes decreases
(b) The mobility of both electrons and holes decreases
(c) The hole density actually reduces
(d) Effect of reduction in electron due to increase in holes compensates more than the effect of increases in holes on conductivity

41. Assuming that the electron mobility in intrinsic silicon is 1500 cm^2/ Vs at room temperature (T = 300K) and the corresponding volt equivalent of temperature V_T = 25.9 mV, what is the approximate value of the electron diffusion constant?

(a) 40 cm^2/ s (b) 4 cm^2/ s

(c) 400 cm^2/ s (d) 4000 cm^2/ s

42. An intrinsic semiconductor with energy gap 1 eV has a carrier concentration N at temperature 200 K. Another intrinsic semiconductor has the same value of carrier concentration N at temperature 600 K. What is the energy gap value for the second semiconductor?

(a) (1 / 3) eV (b) (3 / 2) eV

(c) 3 eV (d) 9 eV

43. Consider the following statements:
n – type of silicon can be
1. formed by adding impurity of phosphorous
2. Formed by adding impurity of arsenic
3. Formed by adding impurity of boron
4. Formed by adding impurity of aluminum

Which of the statements given above are correct?

(a) 1 and 3 only (b) 3 and 4 only
(c) 1 and 2 only (d) 1 ,2,3 and 4

KEY:

1.a	2.a	3.d	4.d	5.d	6.c
7.b	8.b	9.b	10.d	11.d	12.d
13.a	14.b	15.c	16.b	17.d	
18.c	19.d	20.d	21.c	22.c	23.b
24.d	25.c	26.d	27.d	28.b	29.a
30.a	31.a	32.b	33.a	34.d	35.b
36.c	37.b	38.d	39.c	40.b	41.a
42.a	43.c				

PREVIOUS GATE QUESTIONS:

1. n-type silicon is obtained by doping silicon with **GATE - 2003**

(a) Germanium (b) Aluminium
(c) Boron (d) Phosphorus

2. The bandgap of silicon at 300 K is **GATE - 2003**

(a) 1.369 eV (b) 1.10 eV
(c) 0.80 eV (d) 0.67 eV

3. The intrinsic carrier concentration of silicon sample at 300 K is 1.5 X $10^{16}/m^3$. If after doping, the number of majority carriers is 5 X $10^{20}/m^3$, the minority carrier density is **G – 2003**

(a) 4.50 X $10^{11}/m^3$ (b) 3.33 X $10^{4}/m^3$
(c) 5.00 X $10^{20}/m^3$ (d) 3.00 X $10^{-5}/m^3$

4. The bandgap of Silicon at room temperature is **GATE – 2005**

(a) 1.3 eV (b) 0.7 eV
(c) 1.1 eV (d) 1.4 eV

5. The concentration of minority carriers in an extrinsic semiconductor under equilibrium is **GATE – 2006**

(a) directly proportional to the doping concentration
(b) inversely proportional to the doping concentration
(c) directly proportional to the intrinsic concentration
(d) inversely proportional to the intrinsic concentration

6. The electron and hole concentrations in an intrinsic semiconductor are n_i percm^3 at 300 K. Now, if acceptor impurities are introduced with a concentration of N_A per cm^3 (where $N_A >> n_i$) the electron concentration per com^3 at 300 K will be **G - 2007**

(a) n_i (b) $n_i + N_A$

(c) $N_A - n_i$ (d) n_i^2 / N_A

7. An n-type silicon bar 0.1 cm long and 100 μm^2 in cross-sectional area has a majority carrier concentration of 5 x $10^{20}/m^3$ and the carrier mobility is 0.13 m^2/V-s at 300K. If the charge of an electron is 1.6 x 10^{-19} coulomb, the resistance of the bar is **G – 2003**
(a) 10^6 ohm (b) 10^1 ohm
(c) 10^{-1} ohm (d) 10^{-4} ohm

8. The electron concentration in a sample of uniformly doped n-type silicon at 300K varies linearly from $10^{17}/cm^3$ at x = 0 to 6 x $10^{16}/cm^3$ at x = 2 μm. Assume a situation that electrons are supplied to keep this concentration gradient constant with time. If electronic charge is 1.6 x 10^{-19} Coulomb and the diffusion constant D_n = 35cm^2/s, the current density in the silicon, if no electric field is present, is **GATE – 2003**
(a) zero (b) –1120 A/cm^2
(c) –560 A/cm^2 (d) +1120 A/cm^2

9. The resistivity of a uniformly doped n-type silicon sample is 0.5Ω–cm. If the electron mobility (μ_n) is 1250 cm^2/V–sec and the charge of an electron is 1.6 x 10^{-19} Coulomb, the donor impurity concentration (N_D) in the sample is **GATE - 2004**
(a) 2 x $10^{16}/cm^3$ (b) 1 x $10^{16}/cm^3$
(c) 2.5 x.$10^{15}/cm^3$ (d) 2 x $10^{15}/cm^3$

10. A Silicon sample A is doped with 10^{18} atoms/cm^3 of Boron. Another sample B of identical dimensions is doped with 10^{18} atoms/cm^3 of Phosphorus. The ratio of electron to hole mobility is 3. The ratio of conductivity of the sample A to B is **GATE – 2005**
(a) 3 (b) 1/3
(c) 2/3 (d) 3/2

11. The majority carriers in an n-type semiconductor have an average drift velocity v in a direction perpendicular to a uniform magnetic field B. The electric field E induced due to Hall effect acts in the direction **GATE – 2006**
(a) v x B (b) B x v
(c) along v (d) opposite to v

12. A heavily doped n-typed semiconductor has the following data:
Hole-electron mobility ratio : 0.4
Doping concentration : 4.2 x 10^8 atoms/m^3
Intrinsic concentration : 1.5 x 10^4 atoms/m^3
The ration of conductance of the n-type semiconductor to that of the intrinsic semiconductor of same material and at the same temperature is given by **GATE - 2006**
(a) 0.00005 (b) 2,000
(c) 10,000 (d) 20,000

13. Silicon is doped with boron to a concentration of 4 x 10^{17} atoms/cm^3. Assume the intrinsic carrier concentration of silicon to be 1.5 x $10^{10}/cm^3$ and the value of kT/q to be 25mV at 300K. Compared to undoped silicon, the Fermi level of doped silicon **GATE - 2008**
(a) goes sown by 0.13 eV
(b) goes up by 0.13 eV
(c) goes down by 0.427 eV
(d) goes up by 0.427 eV

14. In a n- type silicon crystal at room temperature, which of the following can have a concentration of 4 ×10^{19} cm^{-3}? **G-2009**
a) Silicon atoms
b) Holes
c) Dopant atoms
d) Valence electrons

15. The ratio of the mobility to the diffusion coefficient in a semiconductor has the units **G-2009**
a) V^{-1} b) cm . V^{-1}
c) V . cm^{-1} d) V . s

KEY:

1.d	2.b	3.a	4.c	5.b	6.d
7.a	8.b	9.b	10.b	11.b	12.d
13.c	14.	15.			

CHAPTER - 2 P –N JUNCTION THEORY AND CHARACTERISTICS

(JUNCTION theory, different types of diodes and their characteristics)

SEMICONDUCTOR DIODE CHARACTERISTICS

- The p- and n-type silicon or germanium can be obtained by adding appropriate acceptor or donor impurity into Si or Ge-melt while growing a crystal.
- These crystals are cut into thin slices called 'Wafers'. Semiconductor devices are usually made on these wafers.
- These are many methods of making a p-n junction as given below.
  (a) 'Alloying' technique (b) Diffusion technique
  (c) Vapour deposition (epitaxial growth) and (d) Rate growth junction.
- The donor ion is indicated schematically by a plus sign (+) because, after this impurity atom "donates" an electron it becomes a positive ion. The acceptor ion is indicated by a minus sign
- (-) because, after this atom "accepts" an electron, it becomes a negative ion.
- Initially, there are nominally only p-type carriers to the left of the junction and only n-type carriers to the right.
- Because, there is a density gradient across the junction holes will diffuse to the right across the junction and electrons to the left.
- As a result of the displacement of these carriers, an electric field will appear across the junction. Equilibrium will be established when the field becomes large enough to restrain the process of diffusion.
- The un neutralized ions in the neighborhood of the junction are referred to as "uncovered charges". Since the region of the junction is depleted of mobile charges, it is called the "depletion region, the space-charge region, or the transition region".
- The thickness of this region is of the order of 10^{-4} cm = 10^{-6} m = 1 micron
- The general shape of the charge distribution may be as shown in figure 1.1b.
- The electric field intensity in the neighborhood of the junction is indicated in fig 1.1c.
- The electrostatic-potential variation in the depletion region is shown in fig 1.1d.
- This variation constitutes a potential energy barrier against the further diffusion of holes across the barrier.
- The form of the potential energy barrier against the flow of electrons from the n-side across the junction as shown in fig 1.1e.
- The potential barrier (or field across the junction) and the depletion layer width (or junction width) depends upon the doping concentration on the two sides.

- At equilibrium, there is no net current flowing across the p-n junction.
- The current due to the drift of carriers in the electric field must exactly cancel the diffusion current. $J_p(\text{drift}) + J_p(\text{diffusion}) = 0$

  $$J_n(\text{drift}) + J_n(\text{diffusion}) = 0$$

  Since the net hole current density is zero, the negative of the hole diffusion current must equal the hole drift current. $eD_p \frac{dp}{dx} = e\mu_p p\varepsilon$

  The potential barrier V_0 called the contact, or diffusion, potential is of the order of magnitude of a few tenths of a volt.
- $\nabla^2 V = d^2V/dx^2 = -\rho/\varepsilon$ → Poisson equation is satisfied inside the junction.
- $\nabla^2 V = d^2V/dx^2 = 0$ → Laplace equation is satisfied outside the junction.

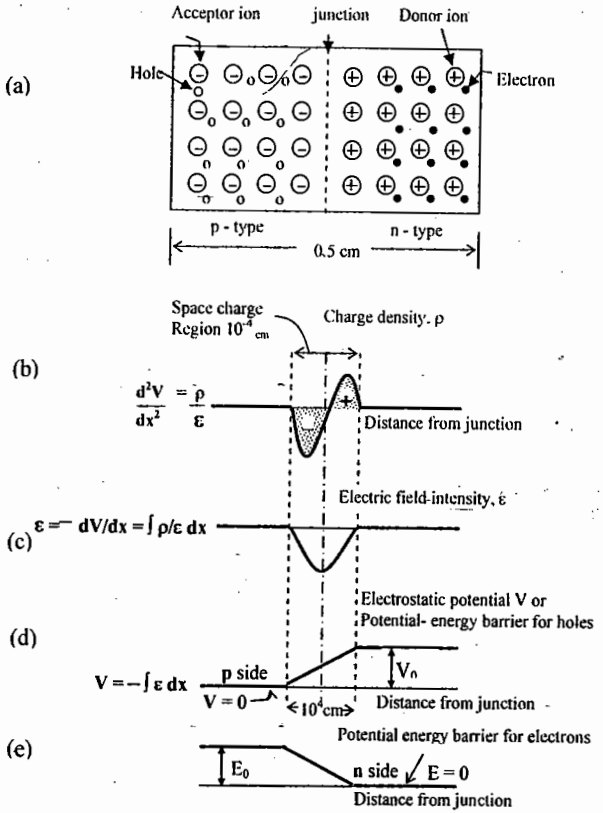


Fig - 1: A schematic diagram of a p – n junction, including the charge density, electric field intensity, and potential – energy barriers at the junctions. (not drawn to scale.)

THE P-N JUNCTION AS A DIODE

- Diode permits the easy flow of current in one direction but restrains the flow in the opposite direction.

Forward Bias:

- Suppose we apply a voltage V such that n-side is negative and p-side is positive.
- The applied voltage V (or bias V) is opposite to the junction barrier potential V.
- The consequences of this are:
  (i) The effective barrier potential becomes ($V_0 - V$) and hence the energy barrier across the junction decreases.
  (ii) more majority carriers will be allowed to flow across the junction.
  (iii) the junction width decreases.
  The current flow is principally due to majority charge carriers and is large (mA).

Reverse Bias:

- The applied voltage V on the n-side is positive and is negative on the p-side.
- The applied bias V and the barrier potential V_0 are in the same direction making the effective junction potential as $V + V_0$. As a result, the junction width will increase.
- The higher junction potential would restrict the flow of majority carriers to a much greater extent.
- However, such a field will favour the flow of minority carriers (as they have opposite charges).
- So, the reverse bias current will be due to the minority carriers only.
- Since, the number of minority carriers is very small as compared to the majority carriers, the reverse bias current is small ($\approx \mu A$).

THE SHORT-CIRCUITED AND OPEN-CIRCUITED P-N JUNCTION:

- If the voltage V applied to the p-n junction is set equal to zero, the p-n junction would be short-circuited.
- Under this condition, no current can flow ($I = 0$) and the electrostatic potential V_0 remains uncharged and equal to the value under open circuit conditions.
- The sum of the voltages around the closed loop must be zero, the junction potential V_0 must be exactly compensated by the metal to semiconductor contact potentials at the ohmic contacts.
- It is not possible to measure contact difference of potential directly with a voltmeter across an open-circuited p-n junction diode and the voltmeter would read zero voltage.

BAND STRUCTURE OF AN OPEN CIRCUITED P-N JUNCTION:

- The Fermi level must be constant throughout the specimen at equilibrium.
- The Fermi level E_F is closer to the conduction band edge E_{cn} in the n-type material and closer to the valence band edge E_{vp} in the p-side.
- The conduction band edge E_{cp} in the p material cannot be at the same level as E_{cn}, nor can the valence band edge E_{vn} in the n-side line up with E_{vp}. Hence the energy band diagram for a p-n junction appears as shown in fig.2 Where a shift in energy levels E_0 is indicated. Note that

$$E_0 = E_{cp} - E_{cn} = E_{vp} - E_{vn} = E_1 + E_2$$

This energy E_0 represents the potential energy of the electrons at junction.

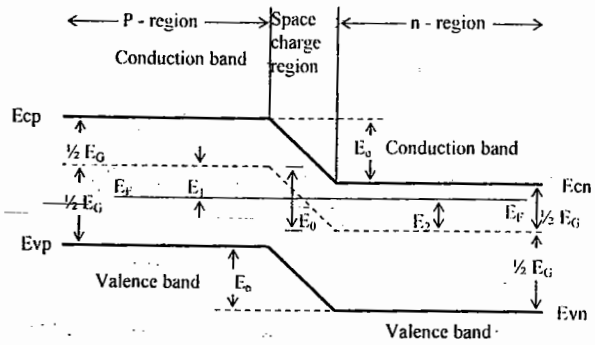


Fig - 2: Band diagram for a p-n junction under open-circuit conditions. This sketch corresponds to fig (1e) and represents potential energy for electrons. The width of the forbidden gap is E_G in electron volts.

From figure,

$E_F - E_{Vp} = 1/2\ E_G - E_1$ **and** $E_{Cn} - E_F = 1/2\ E_G - E_2$ E_G = **forbidden energy gap**

By adding the above equations

$$E_0 = E_1 + E_2 = E_G - (E_{Cn} - E_F) - (E_F - E_{Vp})$$

$$\boxed{E_G = kT \ln [(N_C N_V) / n_i^2]} \quad \text{--- (1)}$$

$$\boxed{E_{Cn} - E_F = kT \ln (N_C / N_D)} \quad \text{--- (2)} \quad \therefore KT = 26\ meV$$

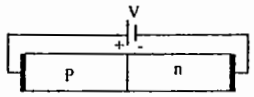
$$\boxed{E_F - E_{Vp} = kT \ln (N_V / N_A)} \quad \text{--- (3)}$$

The E's are expressed in electron volts and k has the dimensions of electron volts per degree Kelvin. The Contact difference in potential V_0 is expressed in volts and is numerically equal to E_0 and it is depends only upon the equilibrium concentrations, and not at all upon the charge density in the transition region(space charge region).
Other expressions for E_0 are

$$\boxed{E_0 = kT \ln \frac{N_D N_A}{n_i^2} = kT \ln \frac{p_{po}}{p_{no}} = kT \ln \frac{n_{no}}{n_{po}}} \quad \text{--- (4)}$$

Rewriting the above equation (4) in another form

$$p_{p0} = p_{n\,o}\, e^{V_0/V_T}$$
$$n_{no} = n_{po}\, e^{V_0/V_T} \quad \text{---} \quad (5)$$



Since $V_0 / V_T = E_0/kT$

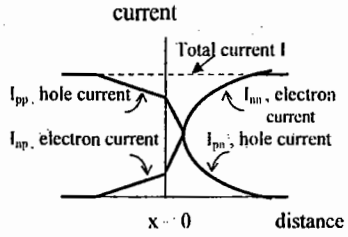


Fig -- 3: The hole and electron-current components vs, distance in a p-n junction diode. The space-charge region at the junction is assumed to be negligibly small.

THE CURRENT COMPONENTS IN A P-N DIODE

- When a forward bias is applied to a diode, holes are injected into the n-side and electrons into the p-side.
- The number of these injected minority carriers falls off exponentially with distance from the junction as shown in fig.(3)
- The symbol $I_{pn}(x)$ represents the hole current in the n material, and $I_{np}(x)$ indicates the electron current in the p-side as a function of **x.**
- Electrons crossing the junction at $x = 0$ from right to left constitute a current in the same direction as holes crossing the junction from left to right.

  Hence the total current **I** at $x = 0$ is

$$I = I_{pn}(0) + I_{np}(0)$$

- Consequently, in the p-side, there must be a second component of current I_{pp} which, when added to I_{np}, gives the total current **I.** Hence this hole current in the p-side I_{pp}(a majority carrier current) is given by

$$I_{pp(x)} = I - I_{np(x)}$$

- This current is plotted as a function of distance as shown in fig.(3) as is also the corresponding electron current I_{nn} in the n material.
- For an un symmetrically doped diode, $I_{pn} \neq I_{np}$.
- The current in a **p-n** diode is bipolar in character since it is made up of both positive and negative carriers of electricity.
- The total current is constant throughout the device, but the proportion due to holes and that due to electrons varies with distance.

QUANTITATIVE THEORY OF THE P-N DIODE CURRENTS

If the forward bias is applied to the diode, holes are injected from the p side into the **n** material. The concentration p_n of holes in the n-side is increased above its thermal equilibrium value p_{no} and, is given by

$$p_n(x) = p_{no} + P_n(0)\, e^{-x/L_p} \quad \text{----} \quad (6)$$

Where the parameter L_p is called the diffusion length for holes in the **n** material.

And the injected or excess concentration at $x = 0$ is

$$P_n(0) = p_n(0) - p_{no}$$

The diffusion hole current in the n-side is given by

$$I_{pn} = -Aq\, D_p \frac{dp_n}{dx} \quad \text{----} \quad (7)$$

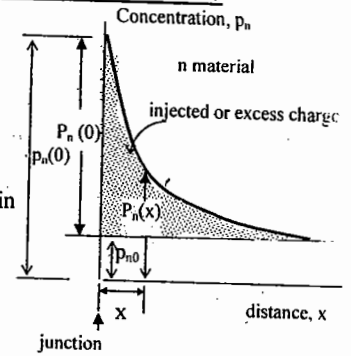


Fig – 4: Defining the several components of hole concentration in the n side of a forward – biased diode.

Taking the derivative of equation (6) and substituting in equation (7) we obtain

$$I_{pn}(x) = \frac{Aq\, D_p P_n(0)}{L_p}\, e^{-x/L_p} \quad \text{----} \quad (8)$$

This equation verifies that the hole current decreases exponentially with distance.

Where q=charge of an electron

THE LAW OF THE JUNCTION

- If the barrier potential across the depletion layer is V_B, then

$$p_p = p_n\, e^{V_B/V_T} \quad \text{---} \quad (9)$$

This is the Boltzmann relationship of kinetic gas theory.

- If we apply above equation to the case of an open-circuited p-n junction, then $p_p = p_{po}$, $p_n = p_{n0}$ and $V_B = V_0$.
- Consider now a junction biased in the forward direction by an applied voltage V.
- Then the barrier voltage V_B is decreased from its equilibrium value V_0 by the amount V or

$$V_B = V_0 - V$$

V_0 = equilibrium value

At the edge of the depletion layer, $x = 0$, $p_n = p_n(0)$, then the above equation(9) is

$$p_{p0} = p_n(0)\, e^{(V_0 - V)/V_T} \quad \text{---} \quad (10)$$

Combining this equation with the above said equation(5), i.e., $p_{p0} = p_{n0} e^{V_o/V_T}$
We obtain,

$$\boxed{p_n(0) = p_{n0} e^{V/V_T}} \quad \text{---} \quad (11)$$

This boundary condition is called the "law of the junction". It indicates that, for a forward bias ($V > 0$), the hole concentration $p_n(0)$ at the junction is greater than the thermal-equilibrium value p_{n0}.

A similar equation, valid for electrons, is obtained by interchanging p and n in above equation(11).

The hole concentration $P_n(0)$ injected into the n-side at the junction is given by

$$P_n(0) = p_{n0} (e^{V/V_T} - 1) \quad \text{.....(12)}$$

THE FORWARD CURRENTS:

- The hole current $I_{pn}(0)$ crossing the junction into the n-side at $x = 0$ is given by

$$I_{pn}(0) = \frac{AqD_p p_{n0}}{L_p} (e^{V/V_T} - 1)$$

- The electron current $I_{np}(0)$ crossing the junction into the p-side is obtained from above equation by interchanging n and p, or

$$I_{np}(0) = \frac{AqD_n n_{p0}}{L_n} (e^{V/V_T} - 1)$$

The total diode current I is the sum of $I_{pn}(0)$ and $I_{np}(0)$, or

$$I = I_0 (e^{V/V_T} - 1)$$

$$\text{where} \quad I_0 = \frac{AqD_p p_{n0}}{L_p} + \frac{AqD_n n_{p0}}{L_n}$$

Hence I_0 is called the "reverse saturation current" and depends on doping concentration.

$$I_0 = Aq\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right) n_i^2 \qquad p_{no} = \frac{n_i^2}{N_D}$$

Where $n_i^2 = A_0 T^3 e^{-E_{GO}/kT} = A_0 T^3 e^{-V_{GO}/kT}$ $\qquad n_{po} = n_i^2 / N_A$

In other form,

$$I_0 = Aq\, n_i^2\, V_T\left(\frac{\mu_p}{L_p N_D} + \frac{\mu_n}{L_n N_A}\right)$$

From Einstein equation, $D_p/\mu_p = D_n/\mu_n = V_T$

$$I_0 = Aq^2 n_i^2 V_T \mu_n \mu_p \left(\frac{1}{L_p \sigma_n} + \frac{1}{L_n \sigma_p}\right)$$

where, $\sigma_n = N_D \mu_n q$ and $\sigma_p = N_A \mu_p q$

V_{GO} is a voltage which is numerically equal to the forbidden gap energy in electron volts. If we consider the recombination of carriers, then the total current I

$$I = I_0(e^{V/\eta V_T} - 1) \quad \text{.....(13)}$$

Where $\eta \approx 2$ for small (rated) currents and $\eta \approx 1$ for large currents.

$\eta \simeq 2$ for silicon

$\eta \simeq 1$ for germanium

- I_0 depends on material and it is fixed for a given device. But varies with temperature

$$I_{o2} = I_{o1} \times 2^{|(T_2 - T_1)/10|} \quad \text{.....(14)}$$

- Where I_{o1} (I_{o2}) is the reverse saturation current at a temperature T_1 (T_2).
- I_0 doubles for every 10°C rise in temperature. That is, it increases 7% / °C.
- I_0 is in the range of microamperes for a germanium diode and nano amperes for a silicon diode.
- Since $n = 2$ for small currents in silicon, the current increases as $e^{V/2V_T}$ for the first several tenths of a volt and increases as e^{V/V_T} only at higher voltages.

THE VOLT-AMPERE CHARACTERISTIC:

For a p-n junction, the current I is related to the voltage V by the equation

$I = I_0(e^{V/\eta V_T} - 1)$ --- (13) $\qquad \eta \simeq 1$ for Ge

$\eta \simeq 2$ for Si

$V_T = T / 11{,}600 = 26$ mV at $T = 300$°K.

At room temperature,

(a) When the voltage V is positive and several times V_T, the unity in the paranthesis of equation (13) may be neglected. i.e., $e^{V/\eta V_T} >> 1$,

$$\therefore I = I_0 e^{V/\eta V_T}$$

Accordingly except for a small range in the neighborhood of the origin, the current increases exponentially with voltage.

(b) When the diode is reverse-biased and |V| is several times V_T, $I \approx -I_0$. The "reverse current" is therefore constant, independent of the applied reverse bias. Consequently, I_0 is referred to as the "reverse saturation current"

At a reverse biasing voltage V_Z, the diode characteristic exhibits an abrupt and marked departure from equation (13). At this critical voltage a large reverse current flows, and the diode is said to be in the "break down region".

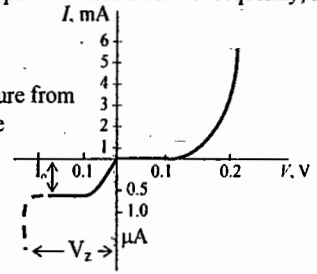


Fig – 5: The volt-ampere characteristic for a germanium diode.

The Cutin Voltage, Offset, break-point, or threshold voltage ($V\gamma$):

Below $V\gamma$ the current is very small (say, less than 1 per cent of max. rated voltage). Beyond $V\gamma$ the current rises very rapidly. $V\gamma = 0.2$ V for Ge, 0.6V for Si.

The reverse saturation current I0 in a Ge is normally larger by a factor of about 1000 than the I0 in a silicon diode of comparable ratings. Since n = 2 for small currents in Si, the I increases as $e^{V/2V_T}$ only at higher voltages.

The resistance R, cutin voltage $V\gamma$, power dissipation and noise margin of Germanium is less than the silicon. But Germanium is not used in switching characteristics.

The temperature dependence of p-n diode characteristics:

The dependence of I0 on temperature T is given approximately by

$$I_0 = kT^m e^{-V_{GO}/\eta V_T}$$

Where k is constant and qV_{GO} (q is the magnitude of the electron charge) is the forbidden gap energy in Joules:

For Ge : n = 1 m = 2 $V_{GO} = 0.785V$

For Si : n = 2 m = 1.5 $V_{GO} = 1.21V$

Taking the derivative of the logarithm of above equation, we find

$$\frac{1}{I0}\frac{dI_0}{dT} = \frac{d}{dT}(\ln I_0) = \frac{m}{T} + \frac{V_{GO}}{\eta T V_T}$$

At room temperature, $d(\ln I_0)/dT = 0.08$ /°C for Silicon and 0.11 / °C for Germanium.

The I0 increases approximately 7 percent / °C for both Si and Ge. Since $(1.07)10 \approx 2.0$, we conclude that the "reverse saturation current(Io)" approximately doubles for every 10°C rise in temperature.

Consider a diode operating at room temperature (300°K) and just beyond the $V\gamma$.

Then we find,

$$\frac{dV}{dT} = \begin{cases} -2.1 \text{ mV/°C for Ge} \\ -2.3 \text{ mV/°C for Si} \end{cases}$$

Since these data are based on "average characteristics", it might be well for conservative design to assume a value of

$$dV/dT = -2.5 \text{ mV/°C.} \quad \text{.....(14)}$$

for either Ge or Si at room temperature.

For Germanium, an increase in temperature from room temperature (25°C) to 90°C ,increases the I0 to hundreds of microamperes, although in Silicon at 100°C the I0 has increased only to some tenths of a micro ampere.

DIODE RESISTANCE

The static resistance **R** of a diode is defined as the ratio **V/I** of the voltage to the current. Typical values for a silicon planar epitaxial diode are $V_F = 0.8V$ at $I_F = 10mA$ (corresponding to $R_F = 80\Omega$) and $I_R = 0.1\mu A$ at $V_R = 50V$ (corresponding to $R_R = 500M$).

For small signal operation the dynamic, or incremental, resistance **r** is an important parameter and is defined as the reciprocal of the slope of the volt-ampere characteristic, **r = dV/dI**. The dynamic resistance is not a constant, but depends upon the operating voltage.

The dynamic conductance **g = 1/r** is

$$G = \frac{dI}{dV} = \frac{I_0 e^{V/\eta V_T}}{\eta V_T} = \frac{I + I_0}{\eta V_T}$$

for $|V/\eta V_T| >> 1$, **g** is small and **r** is very large.
For forward bias, $I >> I_0$, and **r** is given by

$$r \approx (\eta V_T)/I \quad \text{.....(15)}$$

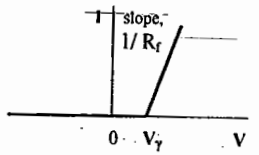


Fig – 6: The piecewise linear characterization of a semiconductor diode.

For an avalanche diode, $V_\gamma = V_Z$, and R_f is the dynamic resistance in the breakdown region.

Type	Model	Characteristics
Ideal device	Ideal diode	I_D, 0, V_D
Simplified model	V_T, Ideal diode	I_D, 0, V_T, V_D
Piece wise linear model	V_T, r_{av}, Ideal diode	I_D, r_{av}, 0, V_T, V_D

TRANSITION OR SPACE CHARGE (OR DEPLETION REGION) CAPACITANCE (C_T)

The parallel layers of oppositely charged immobile ions on the two sides of the junction form the transition capacitance, C_T, which is given by

$$C_T = (\varepsilon A)/W$$

Where $\varepsilon (= \varepsilon_0 \varepsilon_r)$ is the permittivity of the material, A is the cross-sectional area of the junction and W is the width of the depletion layer over which the ions are uncovered.
The net charge must be zero across the depletion region will satisfy the condition

$$N_A W_p = N_D W_n \quad \text{.....(16)}$$

Where

N_A=acceptor concentration ; N_D=donor concentration;
W_p= width of the depletion region in p-side;
W_n= width of the depletion region in n-side;

The effective barrier potential across the junction is

$$V_B = (qN_A W^2) / 2\varepsilon \quad ....(17)$$ if $N_A << N_D$, then $W_p >> W_n$.

The total depletion width, W is given by

$$W = \left(\frac{2\varepsilon V_B}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) \right)^{1/2} \quad .....(18)$$

where,
$V_B = (V_0 - V)$, V is the applied voltage and V_0 is the barrier potential, or the contact potential.

- When no external voltage is applied, i.e., V = 0, the width of the depletion region of a p n junction diode is of the order of 0.5 microns. The movement of majority carriers across the junction causes opposite charges to be stored at this distance W apart. This depletion region acts as a dielectric between the two conducting p- and n-regions. Therefore, these regions act as a parallel plate capacitor whose transition capacitance C_T is approximately 20 pF with no external bias.

- When forward bias +V is applied, the effective barrier potential, $V_B = [V_0 - (+V)]$, is lowered and hence the width of the depletion region W decreases and C_T increases. Under reverse bias condition, the majority carriers move away from the junction, thereby uncovering more immobile charges. Now the effective barrier potential, $V_B = [V_0 - (-V)]$, is increased and hence, W increase with reverse voltage and C_T decreases correspondingly.

- The values of C_T range from 5 to 200 pF, the larger values being for the high power diodes. This property of voltage variable capacitance with the reverse bias appears in varactors, Vari-caps or volta-caps.

DIFFUSION (OR STORAGE) CAPACITANCE (C_D)

The capacitance that exists in a forward biased junction is called a diffusion or storage capacitance (C_D), whose value is usually much larger than C_T, which exists in a reverse-biased junction. This is also defined as the rate of change of injected charge with applied voltage, i.e., $C_D = (dQ/dV)$, where dQ represents the change in the number of minority carriers stored outside the depletion region when a change in voltage across the diode, dV is applied. Diffusion capacitance C_D is proportional to diode forward current, I. Therefore, $C_D = \tau I / (\eta V_T)$, where τ is the mean life time for holes and electrons. The values of C_D range from 10 to 1000 pF, the larger values being associated with the diode carrying a larger anode current, I.

The effect of C_D is negligible for a reverse-biased p-n junction. As the value of C_D is inversely proportional to frequency, it is high at low frequencies and it decreases with the increase in frequency.

$C_D = (L_p^2 g) / D_p$ $\quad g = dI / dV$ $\quad g$ = conductance
$\tau = L_p^2 / D_p$ $\quad g = I / (\eta V_T)$ $\quad \tau$ = mean life time of carriers.
$C_D = \tau g$ $\quad C_D = \tau I / (\eta V_T)$

For a reverse bias 'g' is very small and C_D may be neglected compared with C_T. For a forward current, C_D is usually much larger than C_T. Despite the large value of C_D, the time constant rC_D may not be excessive because the dynamic forward resistance $r = 1/g$ is small.

$$rC_D = \tau$$

Hence the diode time constant equals the mean lifetime of minority carriers, which lies in range of nanoseconds to hundreds of microseconds.

Charge-Control Description of a Diode:

$$I = (Q D_p) / L_p^2 = Q/\tau$$

This is very important equation states that the diode current is proportional to the stored charge of excess minority carriers.

Thus, in the steady state, the current I supplies minority carriers at the rate at which these carriers are disappearing because of the process of recombination.

DIODE APPLICATIONS

An ideal p-n junction diode is a two terminal polarity sensitive device that has zero resistance (diode conducts) when it is forward biased and infinite resistance (diode does not conduct) when reverse biased. Due to this characteristic the diode finds number of applications as given below.

(i) rectifiers in d.c power supplies
(ii) switch in digital logic circuits used in computers
(iii) clamping network used as d.c restorer in TV receivers and voltage multipliers
(iv) clipping circuits used as wave shaping circuits used in computers, radars, radio and TV receivers.
(v) demodulation (detector) circuits.

The same PN junction with different doping concentration finds special applications as follows:

(i) detectors (APD, PIN photo diode) in optical communication circuits
(ii) Zener diodes in voltage regulators
(iii) varactor diodes in tuning sections of radio and TV receivers
(iv) light emitting diodes in digital displays
(v) LASER diodes in optical communications
(vi) Tunnel diodes as a relaxation oscillator at microwave frequencies.

BREAKDOWN DIODES

Diodes which are designed with adequate power dissipation capabilities to operate in the breakdown region may be employed as voltage-reference or constant voltage devices. Such diodes are known as avalanche, breakdown, or Zener diodes.

The reverse voltage characteristic of a semiconductor diode, including the breakdown region is shown in fig.7 (a). By reverse biasing, the diode is operating in the breakdown region as shown in fig.7 (b)

The diode will regulate the load voltage against variations in load current and against variations in supply voltage V because, in the break down region, large changes in diode current produce only small changes in diode voltage.

The upper limit on diode current is determined by the power dissipation rating of the diode.The thermally generated electrons and holes acquire sufficient energy from the applied potential to produce new carriers by removing valence electrons from their bonds. These new carriers, in turn, produce additional carriers again through the process of disrupting bonds. This cumulative process is referred to as "avalanche multiplication". It results in the flow of large reverse currents, and the diode finds itself in the region of "avalanche breakdown".

Even if the initially available carriers do not acquire sufficient energy to disrupt bonds, it is possible to initiate breakdown through a direct rupture of the bonds because of the existing of the strong electric field. Under these circumstances the break down is referred to as the "zener breakdown".This zener effect is now known to play with breakdown voltages below about 6V.

If the reference voltage is above 6V, where the physical mechanism involved is avalanche multiplication, the temperature coefficient is positive.
However, below 6V, where true zener breakdown is involved, the temperature coefficient is negative.

The zener breakdown voltage decreases with temperature. The value of the avalanche voltage must increase with increased temperature.

The capacitance across a breakdown diode is the transition capacitance. High power avalanche diodes have very large capacitances. C_T is from 10 to 10,000 pf are common.

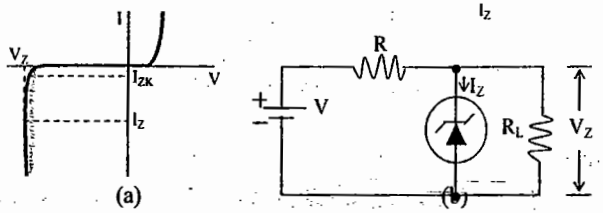


Fig – 7: (a) The volt-ampere characteristic of an avalanche, or Zener, diode.

(b) A circuit in which such a diode is used to regulate the voltage across R_L against changes due to variations in load current and supply voltage.

TUNNEL DIODE

A p-n junction diode has an impurity concentration of about 1 part in 10^8. With this amount of doping, the width of the depletion layer, which constitutes a potential barrier at the junction, is of the order of 5 microns (5×10^{-6} m). If the concentration of impurity atoms is greatly increased, say, to 1 part in 10^3 (corresponding to a density in excess of 10^{19} /cm^3), the device characteristics are completely changed. This new diode was announced in 1958 by Esaki.

Tunneling phenomenon: The width of the junction barrier varies inversely as the square root of impurity concentration and therefore is reduced from 5 microns to less than 100A

(10^{-6} cm). This thickness is only about one-fifth the wavelength of visible light.

Classically, a particle must have energy at least equal to the height of a potential barrier if it is to move from one side of the barrier to the other. However, for barriers as thin as those estimated above in Esaki diode, the Schrodinger equation indicates that there is a large probability that an electron will penetrate through the barrier. This quantum mechanical behavior is referred to as "tunneling", and hence these high-impurity density p-n junction devices are called "tunnel diodes".

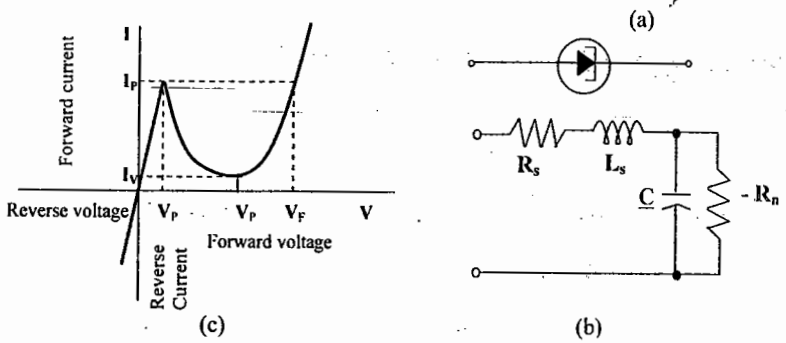


Fig – 8: (a) symbol for a tunnel diode
(b) small-signal model of a tunnel diode in the negative resistance region
(c) the volt-ampere characteristic of a tunnel diode.

Characteristics of a Tunnel Diode:

The tunnel diode exhibits a negative resistance characteristic between the peak current I_p and the minimum value I_v, called the valley current. The tunnel diode useful in pulse and digital circuitry. The small-signal model for operation in negative resistance region is indicated in fig.8.(b)

Tunnel diode is used as very high speed switch. Switching times of the order of a nanosecond are reasonable and times as low as 50 p sec have been obtained. A second application is as a high frequency (microwave) oscillator. The voltages V_v and V_F have negative temperature coefficients of about 1.0 mV/°C.

Tunnel diode Applications:

1. Tunnel diode is used as an ultra-high speed switch, switching speed of the order of ns or ps
2. As logic memory storage device
3. As microwave oscillator
4. In relaxation oscillator circuit
5. As an amplifier.

Advantages

1. Low noise 2. Ease of operation 3. High speed 4. Low power

Disadvantages

1. Voltage range over which it can be operated is 1 V or less.
2. Being a two terminal device, there is no isolation between the input and output circuit.

OBJECTIVES

01. Reverse recovery current in a diode depends on
(a) forward field current
(b) storage charge
(c) temperature
(d) PIV

02. Choose proper substitutes for X and Y to make the following statement correct Tunner diode and Avalanche photodiode are operated in X bias and Y bias respectively.
(a) X:reverse, Y:reverse
(b) X:reverse, Y:forward
(c) X:forward, Y:reverse
(d) X:forward, Y:forward

03. The values of voltage (V_D) across a tunnel diode corresponding to peak and valley currents are V_p and V_v respectively. The range of tunnel diode voltage V_D for which the slope of its I - V_D characteristics is negative would be
(a) $V_D < 0$ (b) $0 \le V_D < V_p$
(c) $V_p \le V_D < V$ (d) $V_D \ge V_v$

04. A tunnel diode is
(a) High resistivity p –n junction diode
(b) A slow switching device
(c) An amplifying device
(d) A very heavily doped p-n diode

05. In a p^+n junction diode under reverse bias, the magnitude of electric field is maximum at
(a) the edge of the depletion region on the p-side
(b) the edge of the depletion region on the n- side
(c) the p^+n junction
(d) the centre of the depletion region on the n- side

06. The junction capacitance of a p-n junction depends on
(a) Doping concentration only
(b) Applied voltage only
(c) Both Doping concentration Applied voltage only
(d) Barrier potential only

07. Under small signal operation of a diode
(a) its bulk resistance increases
(b) its junction resistance predominates
(c) it acts like a closed switch
(d) it behaves as a clipper

08. The reverse current of a silicon diode is
(a) Highly bias voltage sensitive
(b) Highly temperature sensitive
(c) Both bias voltage and temperature sensitive
(d) Independent of bias voltage and temperature

09. In switching diode fabrication, a dopant is introduced into silicon which introduces additional trap levels in the material thereby reducing the mean life time of carriers This dopant is
(a) Aluminium (b) Platinum
(c) Gold (d) Copper

10. The diffusion potential across a p-n junction
(a) decreases with increasing doping concentration
(b) increases with decreasing doping concentration
(c) does not depend on doping concentration
(d) increases with increasing in doping concentration

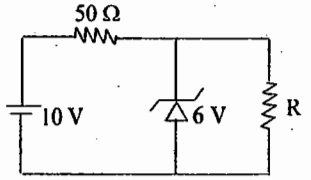
11. The transition region in an open circuited p-n junction contains
(a) free electrons only
(b) holes only
(c) both free electrons and holes
(d) uncovered immobile impurity ions

12. In a p-n diode, hole diffuse from p-region to n-region because
(a) there is higher concentration of holes in p-region
(b) holes are positively charged
(c) holes are urged to move by the barrier potential
(d) the free electrons in the n-region attract the holes

13. In an unbiased p-n junction. the junction current at equilibrium is
(a) due to diffusion of majority carrier
(b) due to diffusion of minority carrier
(c) zero due to equal and opposite currents crossing the junction
(d) zero because no charges cross the junction

14. In an unbiased p-n junction, zero current implies that
(a) the potential barrier has disappeared.
(b) number of holes diffusing from n-side equals the number of electrons diffusing from n-side to p-side
(c) no carrier across the junction.
(d) total current crossing the junction from p-side to n-side equals the total current crossing the junction from n - side to p-side.

15. The 6 V zener diode shown in figure has zero zener resistance and a knee current of 5 mA. The minimum value of R so that the voltage across it does not fall below 6 V is



(a) 1.2 KΩ (b) 80 Ω
(c) 50 Ω (d) 0 Ω

16. The built in potential (diffusion potential) in a p-n junction
(a) is equal to the difference in the fermi level of the two sides, expressed in volts.
(b) increases with the increase in the doping levels of the two sides.
(c) increases with the increase in temperature.
(d) all of above

17. A zener diode works on the principle of
(a) tunneling of charge carriers across the junction
(b) thermionic emission
(c) diffusion of charge carriers across the junction
(d) hopping of charge carriers across the Junction

18. The depletion capacitance C_J of an abrupt p n junction with constant doping on either side varies with reverse bias V_R as
(a) $C_J \propto V_R$ (b) $C_J \propto V_R^{-1}$
(c) $C_J \propto V_R^{-1/2}$ (d) $C_J \propto V_R^{-1/3}$

19. The static characteristic of an adequately forward biased p-n junction is a straight line, if the plot is of
(a) log I Vs log V (b) log I Vs V
(c) I Vs log V (d) I Vs V

20. Silicon diode is less suited for low voltage rectifier operation because
(a) It can withstand high temperatures
(b) Its reverse saturation current is low
(c) Its cut-in voltage is high
(d) Its breakdown voltage is high

21. In a junction diode
(a) The deflection capacitance increases with increases in reverse bias.
(b) The deflection capacitance decrease with increase in reverse bias.
(c) The diffusion capacitance increases with increase in the forward bias.
(d) The diffusion capacitance is much higher than the deflection capacitance when it is forward biased.

22. The depletion region in semiconductor p-n junction diode has
(a) electrons and holes
(b) positive and negative ions on Either side
(c) neither electron nor ion
(d) no holes

23. A p-n junction diode's dynamic conductance is directly proportional to?
(a) the applied voltage
(b) the temperature
(c) its current
(d) the thermal voltage

24. For diode current of 1 mA, at 27°C, a Ge diode requires a forward bias of 0.2165 V where a Si diode requires a FB of 0.872 V. The ratio of reverse saturation current in Ge diode to that in Si diode to the closest approximation is
(a) 1 (b) 3×10^5
(c) 4.7×10^3 (d) 6×10^5

25. The diffusion capacitance of a forward biased p+ - n junction diode with a steady current I depends on
(a) width of the depletion region.
(b) mean lifetime of the holes.
(c) mean lifetime of the electrons.
(d) junction area.

26. Why is an external pass resistor used in a voltage regulator?
(a) For short circuit protection.
(b) For increas ng the current that regulator can andle
(c) For increasing the ou put voltage
(d) For improving the regulation.

27. Two p-n junction diodes are connected back to back to make a transistor Which one of the following is correct?
(a) The current gain of such a transistor will be high
(b) The current gain of such a transistor wil be moderate.
(c) It cannot be used as a transistor due to large base width.
(d) It can be used only for p-n-p transistor

28. What is the reverse recovery t me of a diode when sw tched from forward bias V_F to reverse b as V_R?
(a) Time taken to remove the stored m nority carriers
(b) Time taken by the diode voltage to attain zero value
(c) Time to remove stored minority carriers plus the time to bring the diode voltage to reverse bias V_R
(d) Time taken by the diode current to reverse

29. Match List-I (p-n junction diodes) with List-II (Bias condition) and select the correct answer using the code given below the lists:

List-I	List-II
A. Zener Diode	1. Forward bias
B. Solar cell	2. Reverse bias
C. LASER diode	
D. Avalanche Photodiode	

	A	B	C	D
(a)	1	2	1	2
(b)	2	1	1	2
(c)	2	2	2	1
(d)	2	1	2	2

30. Match List-I (Diode) with List-II (Application) and select the correct answer using the code given below the lists:

List-I
A. Varactor diode
B. Tunnel diode
C. Photodiode
D. Zener diode

List-II
1. To charge auxiliary storage batteries
2. Best choice for silicon ICs
3. Suitable for ICs of III-V
4. High frequency switching circuit

	A	B	C	D
(a)	2	1	4	3
(b)	3	1	4	2
(c)	3	4	1	2
(d)	2	4	1	3

31. Match List-I (Diode type) with List-II (important properties) and select the correct answer using the code given below the lists:

List - I
A. Zener Diode
B. Gunn Diode
C. Schottky Diode
D. Tunnel Diode

List – II
1. Negative resistance device fabricated using semiconductor like Si, Ga, As, Ge etc. can be operated at a frequency of 10GHz
2. Quantum mechanical tunneling with very thin depletion layers under reverse bias operated as a reference voltage sources
3. Negative conductance device, operates on the principle of transfer of electron from one region of conduction band to another
4. Metal – semiconductor diode, have rectification properties

Codes:

	A	B	C	D
(a)	2	4	3	1
(b)	1	3	4	2
(c)	2	3	4	1
(d)	1	4	3	2

32. Match List-I (Devices) with List-II (Property) and select the correct answer using the code given below the lists:

List-I
A. Silicon diode
B. Germanium diode
C. LED
D. PIN diode

List-II
1. High frequency applications
2. Very low reverse bias saturation current
3. Low forward bias voltage drop
4. Cut-off wavelength

Codes:

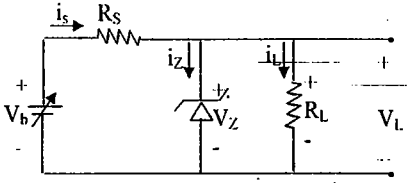
	A	B	C	D
(a)	1	3	4	2
(b)	2	4	3	1
(c)	1	4	3	2
(d)	2	3	4	1

33. In the energy band diagram of an open circuited pn junction, the energy band of n-region has shifted relative to that of p-region.
(a) downward by Eo
(b) upward by Eo
(c) downward by $E_0/2$
(d) upward by $E_0/2$

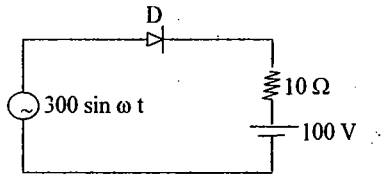
34. A p-n junction in series with a 100Ω resistors, is forward biased so that a current of 100 mA flows. If the voltage across this combination is instantaneously reversed to 10V at t = 0, the reverse current that flows through the diode at t = 0 is approximately given by
(a) 0 mA (b) 100 mA
(c) 200mA (d) 50 mA

35. The change in barrier potential of a silicon p – n junction with temperature is
(a) 0.025 volts per degree C
(b) 0.250 volts per degree C
(c) 0.030 volts per degree C
(d) 0.014 volts per degree C

36. Consider the following circuit

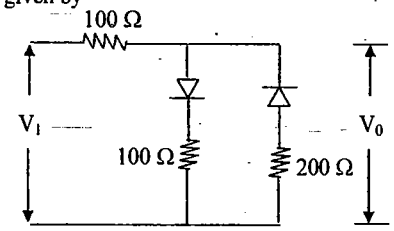


Zener diode has zener voltage $V_Z = 16$ V at a minimum i_Z of 15 mA.



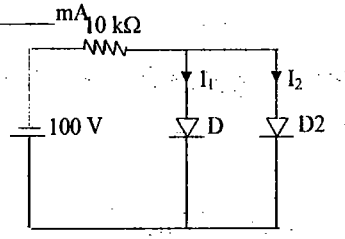
If $V_b = 24 \pm 3$ V and R_L varies from 250 Ω to 2 k Ω, Find the value of R_S to maintain regulation
(a) $R_S > 55.92$ (b) $R_S < 123.04$
(c) $R_S < 63.29$ (d) $R_S > 23.8$

37. For the circuit shown below V_4 is given by $(2 + 0.1 \sin \omega t)$ volts. Assuming $V_D = 0.7$ V and diode as linear device the output voltage V_0 is given by



(a) 0.59 sin ωt V
(b) 0.36 + 0.59 sin ωt V
(c) 0.94 + 0.04 sin ωt V
(d) 1.2 + 0.63 sin ωt V

38. Each diode in figure can be described by a cut – in voltage and zero resistance. If the cut – in voltage of diode D1 is 0.2 V and of diode D2 is 0.6 V, the magnitude of current I_1 through D1 is _____ mA and magnitude of current through D2 is _____ mA

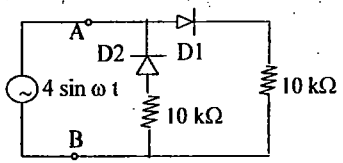


(a) 20 mA, 0 mA (b) 10 mA, 0 mA
(c) 15 mA, 0 mA (d) 25 mA, 0mA

39. In figure, PIV required for the diode is

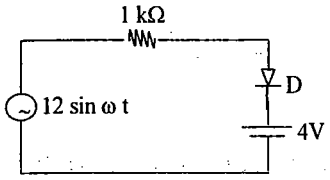
(a) 300 V (b) 100 V
(c) 200 V (d) 400 V

40. A voltage $v = 4 \sin \omega t$ is applied to the terminals A and B of the circuit shown in figure. The diodes are assumed to be ideal. The impedance offered by the circuit across the terminals A and B in kilo ohms is



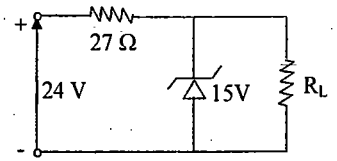
(a) 5 (b) 20
(c) 10 (d) None of these

41. The peak current through the resistor of circuit of figure, assuming the diodes to be ideal, is



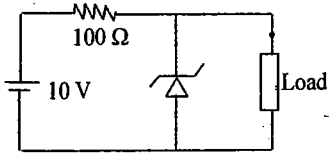
(a) 12 mA (b) 4 mA
(c) 16 mA (d) 8 mA

42. The circuit in figure shows zener – regulated dc power supply. The zener – diode is ideal. The minimum value of R_L down to which the output voltage remains constant is



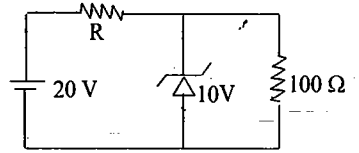
(a) 27 Ω (b) 45 Ω
(c) 15 Ω (d) 24 Ω

43. In the circuit of figure, the 5 V zener diode requires a minimum current of 10 mA. For obtaining a regulated output of 5 V, the maximum permissible load current I_L is _____ mA and the minimum power rating of zener diode is ___W.



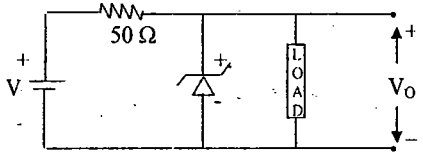
(a) 40 mA and 0.05 W
(b) 10 mA and 0.20 W
(c) 25 mA and 0.10 W
(d) 5 mA and 0.15 W

44. Figure shows an electronic voltage regulator. The Zener diode may be assumed to require a minimum current of 25 mA for satisfactory operation. The value of R required for satisfactory operation is _____ ohms.



(a) 50 Ω (b) 20 Ω
(c) 80 Ω (d) 35 Ω

45. A zener diode in the circuit shown in the figure below, has knee current of 5mA and a maximum allowed power dissipation of 300mw. What are the minimum and maximum load currents that can be drawn safely from the circuit, keeping the output voltage V_0 at 6 V?



(a) 0 mA, 180 mA (b) 5 mA, 110 mA
(c) 10 mA, 55 mA (d) 60 mA, 180mA

KEYS :

01 a	02. c	03.c	04.d	05.c	06.c
07.b	08.b	09.a	10.d	11.d	12.a
13.c	14.d	15.b	16.d	17.a	18.c
19.b	20.d	21.b	22.b	23.c	24.c
25.b	26.a	27.c	28.a	29.b	30.c
31.c	32.d	33.a	34.b	35.a	36.c
37.c	38.b	39.b	40.c	41.d	42.b
43.a	44.c	45.c			

PREVIOUS IES QUESTIONS:

01. A p-n junction diode's dynamic conductance is directly proportional to
(a) the applied voltage
(b) the temperature
(c) its current
(d) the thermal voltage

02. The AC resistance of a forward-biased p-n junction diode operating at a bias voltage 'V' and carrying current 'I' is
(a) zero
(b) a constant value independent of V and I
(c) V/I
(d) $\Delta V / \Delta I$

03. Match **List-I** (Devices) with **List-II** (Property) and select the correct answer using the codes given below the lists:

List-I
A. Silicon diode
B. Germanium diode
C. LED
D. PIN diode

List-II
1. High frequency applications
2. Very low reverse bias saturation current
3. Low forward bias voltage drop
4. Cut-off wavelength

Codes:

	A	B	C	D
(a)	1	3	4	2
(b)	2	4	3	1
(c)	1	4	3	2
(d)	2	3	4	1

04. The depletion layer across a p^+-n junction lies
(a) mostly in the p^+ – region
(b) mostly in the n – region
(c) equally in both the p^+ and n – regions
(d) entirely in the p^+ – regions

05. **Assertion (A):** The diode current is controlled by minority carrier injection over a potential barrier. In the forward bias condition, the minority carriers are increased exponentially.
Reason(R): At high forward bias, the electric field in the neutral regions is no longer negligible as the minority charge density approaches the majority charge density. The diode starts to behave like an ohmic device.
(a) Both A and R are true and R is the correct explanation of A.
(b) Both A and R are true but R is NOT the correct explanation of A.
(c) A is true but R is false.
(d) A is false but R is true.

06. Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I
A. Zener Diode
B. Gunn Diode
C. Schottky Diode
D. Tunnel Diode

List-II
1. Negative resistance device fabricated using semiconductors like Si, GaAs, Ge etc. can be operated at a frequency of 10 GHz.
2. Quantum mechanical tunneling with very thin depletion layers under reverse bias operated as a reference voltage sources.
3. Negative conductance device, operates on the principle of transfer of electron from one refion of conduction band to another.
4. Metal – semiconductor diode, have rectification properties.

Codes:

	A	B	C	D
(a)	2	4	3	1
(b)	1	3	4	2
(c)	2	3	4	1
(d)	1	4	3	2

07. The change in barrier potential of a silicion P-N junction with temperature is
(a) 0.0025 Volts per degree C
(b) 0.0250 Volts per degree C
(c) 0.0030 Volts per degree C
(d) 0.0014 Volts per degree C

08. The diffusion capacitance of a p-n junction diode
(a) increases exponentially with forward bias voltage.
(b) Decreases exponentially with forward bias voltage.
(c) Decreases linearly with forward bias voltage.
(d) Increases linearly with forward bias voltage.

09. The reverse current of a silicon diode is
(a) Highly bias voltage sensitive.
(b) Highly temperature sensitive.
(c) Both bias voltage and temperature sensitive
(d) Independent of bias voltage and temperature.

10. Depletion capacitance in a diode depends on
1. Applied junction voltage
2. Junction built-in potential
3. Current through junction
4. Doping profile across the junction
Select the correct answer using the codes given below
(a) 1 and 2 (b) 1 and 3
(c) 1, 2 and 4 (d) 2, 3 and 4

11. The depletion region in a semiconductor p-n junction diode has
(a) Electrons and holes
(b) Positive and negative ions on either side
(c) Neither electrons nor ions.
(d) No holes.

12. When a junction diode is used in switching applications, the forward recovery time is
(a) of the order of the reverse recovery time
(b) negligible in comparison to the reverse recovery time.
(c) greater than the reverse recovery time
(d) equal to the mean carrier life time τ for the excess minority carriers.

13. Which one of the following statement is correct? A tunnel diode is always biased
(a) by a d. c source
(b) in the middle of its negative resistance region
(c) in the positive resistance region nearest to zero
(d) in the reverse direction

14. A tunnel diode is
(a) High resistivity p-n junction diode
(b) A slow switching device
(c) an amplifying device
(d) A very heavily doped p-n junction diode

15. The junction capacitance of a p-n junction depends on
(a) Doping concentration only
(b) Applied voltage only
(c) Both doping concentration and applied voltage
(d) Barrier potential only

16. Match List – I (Diode) with List – II (Common Application) and select the correct answer using the code given below the lists:

List – I

A. Tunnel diode
B. PIN diode
C. Zener diode
D. Photo diode

List – II

1. Reading of film sound track
2. High frequency oscillator circuits
3. Very high frequency switching circuits
4. Reference voltage.

Codes:

	A	B	C	D
(a)	4	3	2	1
(b)	2	1	4	3
(c)	4	1	2	3
(d)	2	3	4	1

17. The doping concentration on the n – side of a p – n junction diode is enhanced. Which one of the following will get affected?
(a) Width of the depletion region on n - side
(b) Width of the depletion region on p - side
(c) Width of the depletion region on both side
(d) No change in width of depletion region

18. In step – graded p – n junction diode, what is the ratio of depletion – region penetration depths into p and n regions (if the ratio of acceptor to donor (if the ratio of acceptor to donor impurity atoms' densities is 1:2)?
(a) 2 : 1 (b) 4 : 1
(c) 1 : 2 (d) 1 : 4

19. What is the typical value for the ratio of current in a p – n junction diode in the forward bias and that in the reverse bias?
(a) 1 (b)10
(c) 100 (d) 1000

20. Consider the following statements for a p – n junction diode:
1. It is an active component.
2. Depletion layer width decreases with forward biasing
3. In the reverse biasing case, saturation current increases with increasing temperature.
Which of the statements given above are correct?
(a) 1 , 2 and 3 (b) 1 and 2 only
(c) 2 and 3 only (d) 1 and 3 only

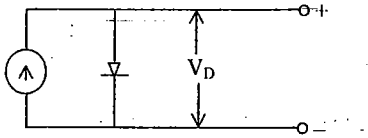
21. Consider the following statements pertaining to tunnel diodes:
1. Impurity concentration is high
2. Carrier velocities are low
3. They have current - controlled V – I characteristic..
Which of the statements (s) given above is/ are correct?
(a) 1 only (b) 2 and 3 only
(c) 1 and 3 only (d) 1 and 2 only

KEY:

1.c	2.d	3.d	4.b	5.c	6.c
7.a	8.a	9.b	10.c	11.b	12.b
13.b	14.d	15.c	16.d	17.a	18.a
19.d	20a	21.a			

PREVIOUS GATE QUESTIONS:

1. In the figure, silicon diode is carrying a constant current of 1 mA. When the temperature of the diode is 20°C, V_D is found to be 700 mA. If the temperature rises to 40°C, V_D becomes approximately equal to **GATE – 2002**



(a) 740 mV (b) 660 mV
(c) 680 mV (d) 700 mV

2. Choose proper substitutes for X and Y to make the following statement correct Tunnel diode and Avalanche photodiode are operated in X bias and Y bias respectively. **GATE - 2003**
(a) X: reverse, Y: reverse
(b) X: reverse, Y: forward
(c) X: forward, Y: reverse
(d) X: forward, Y: forward

3. A Silicon PN junction at a temperature of 20°C has a reverse saturation current of 10 pico-Amperes(pA). The reverse saturation current at 40°C for the same bias is approximately. **GATE – 2005**
(a) 30 pA (b) 40 pA
(c) 50 pA (d) 60 pA

4. The primary reason for the widespread use of Silicon in semiconductor device technology is **GATE – 2005**
(a) abundance of Silicon on the surface of the Earth.
(b) larger bandgap of Silicon in comparison to Germanium.
(c) favorable properties of Silicon-dioxide (SiO_2).
(d) lower melting point.

5. The values of voltage (V_D) across a tunnel-diode corresponding to peak and valley currents are V_p and V_v respectively. The range of tunnel-diode voltage V_D for which the slope of its I–V_D characteristics is negative would be **GATE – 2006**
(a) $V_D < 0$ (b) $0 \le V_D < V_p$
(c) $V_p \le V_D < V_v$ (d) $V_D \ge V_v$

6. In a p^+n junction diode under reverse bias, the magnitude of electric field is maximum at **GATE – 2007**
(a) the edge of the depletion region on the p-side
(b) the edge of the depletion region on the n-side
(c) the p^+n junction
(d) the centre of the depletion region on the n-side.

7. Which of the following is NOT associated with a p-n junction? **GATE - 2008**
(a) Junction Capacitance
(b) Charge Storage Capacitance
(c) Depletion Capacitance
(d) Channel Length Modulation

8. At 300 K, for a diode current of 1 mA, a certain germanium diode requires a forward bias if 0.1435 V, whereas a certain silicon diode requires a forward bias of 0.718V. Under the conditions stated above, the closest approximation of the ratio of reverse saturation current in germanium diode to that in silicon diode is **GATE - 2003**
(a) 1 (b) 5
(c) 4×10^3 (d) 8×10^3

9. In an abrupt p-n junction, the doping concentrations on the p-side and n-side are $N_A = 9 \times 10^{16}/cm^3$ and $N_D = 1 \times 10^{16}/cm^3$ respectively. The p-n junction is reverse biased and the total depletion width is 3μm. The depletion width on the p-side is
GATE – 2004
(a) 2.7μm (b) 0.3μm
(c) 2.25μm (d) 0.75μm

10. A Silicon PN junction diode under reverse bias has depletion region of width 10μm. The relative permittivity of Silicon, $\varepsilon_r = 11.7$ and permittivity of free space $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m,
The depletion capacitance of the diode per square meter is
GATE – 2005
(a) 100μF (b) 10μF
(c) 1μF (d) 20μF

11. A p^+n junction has built-in potential of 0.8V. The depletion layer width at a reverse bias of 1.2 V is 2μm. For a reverse bias of 7.32 V, the depletion layer width will be
GATE - 2007
(a) 4 μm (b) 4.9 μm
(c) 8 μm (d) 12 μm

12. Consider the following assertions.
S1: For Zener effect to occur, a very abrupt junction is required
S2: For quantum tunneling to occur, a very narrow energy barrier is required.
Which of the following is correct?
GATE - 2008
(a) Only S2 is true
(b) S1 and S2 are both true but S2 is not a reason for S1
(c) S1 and S2 are both true and S2 is a reason for S1
(d) Both S1 and S2 are false.

Common Data for Questions 13 and 14:

Consider a silicon p-n junction at room temperature having the following parameters:
Doping on the n-side = 1×10^{17} cm^{-3}
Depletion width on the n-side = 0.1 μm
Depletion width on the p-side = 1.0 μm
Intrinsic carrier concentration = 1.4×10^{10} cm^{-3}
Thermal voltage = 26 mV
Permittivity of free space = 8.85×10^{-14} F. cm^{-1}
Dielectric constant of silicon = 12

13. The built- in potential of the junction
a) is 0.70 V
b) is 0.76 V
c) is 0.82 V
d) cannot be estimated from the data given.

14. The peak electric field in the device is
0a) 0.15 MV . cm^{-1}, directed from p - region to n- region.
b) 0.15 MV . cm^{-1} directed from n - region to p- region.
c) 1.80 MV . cm^{-1} directed from p - region to n- region.
d) 1.80 MV . cm^{-1} directed from n - region to p- region.

KEY:

1.b	2.c	3.d	4.a	5.c	6.c
7.d	8.c	9.b	10.b	11.a	12.a
13.	14.				

CHAPTER – 3 TRANSISTOR THEORY (BJT, FET)

TRANSISTOR

Transistor was first invented in 1948 by J. Bardeen and W.H. Brattain of Bell Telephone Laboratories, U.S.A.

It consists of two p-n junctions back-to-back and is obtained by sandwiching either p-type or n-type semiconductor between a pair of opposite type of semiconductors.
Obviously, there are two types of transistors.

(a) p-n-p transistor: Here two blocks of p-type semiconductor termed as emitter and collector are separated by a thin block of n-type semiconductor (termed as base).

(b) n-p-n transistor: Here two blocks of n-type semiconductor (termed as emitter and collector) are separated by a thin block of p-type semiconductor (termed as base).

You will note that all the three blocks of a transistor shown in below fig are not equal. Further, for getting transistor action, the doping levels in the different blocks are kept different as under:

- **Emitter:** This is the left hand block of the transistor. It is of **moderate size** and **heavily doped** semiconductor. This supplies a large number of **majority carriers** for the current flow through the transistor.
- **Base:** This is the central block. **It is very thin** and **lightly doped.**
- **Collector:** This collects a **major** portion of the majority carriers supplied by the emitter. The collector side is **moderately doped** and **larger** in size(to withstand the temperature generated at the collector) as compared to the **emitter.**

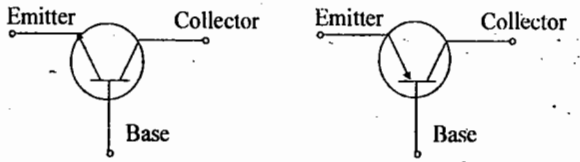


Fig1: Symbols for n-p-n and p-n-p transistor

If the arrow mark is towards the base, it is PNP transistor if it is away then it is NPN transistor.

The arrow mark on the emitter specifies the direction of current when the emitter base junction is forward biased. When the PNP transistor is forward biased; holes are injected into the base. So the holes move from emitter to base.

The conventional current flows in the same direction as holes. So arrow mark is towards the base for PNP transistor. Similarly for NPN transistor, it is away.

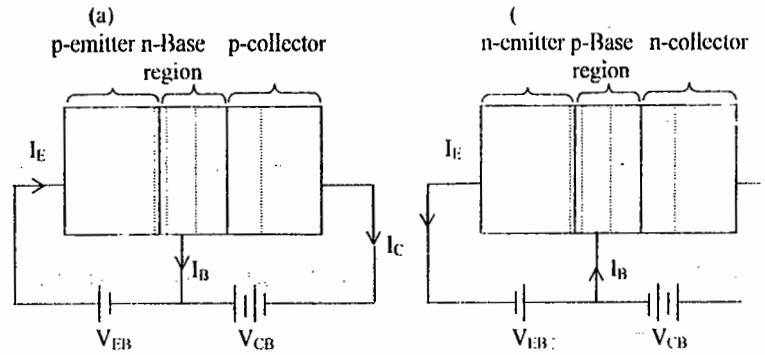


Fig2. Bias Voltage applied : (a) p-n-p transistor and (b) n-p-n transistor.

For understand the action of a transistor, we have to consider the nature of depletion layers formed at the emitter-base p-n junction and base-collector p-n junction.

In general, the *emitter-base junction* of a transistor is forward biased while *collector base junction* is reverse biased as shown in fig2.

This figure also shows the two depletion layers formed at the emitter-base junction and collector-base junction. Since the emitter base junction is forward biased (as well as due to heavy doping of the emitter), this depletion layer will be narrow while the collector-base junction being reverse biased will be relatively wider.

The forward bias voltage V_{EB} is small (0.5 to 1 V) while the reverse bias voltage V_{CB} is considerably high (5 to 15 V).

Consider the case of a biased p-n-p transistor shown in fig2. As the emitter base junction is forward biased, a large number of holes (majority carriers) from p-type emitter block flow towards the base. These constitute the current through the emitter, I_E. These holes have a tendency to combine with the electrons in the base-region (giving only a very small base current, I_B) **because the base is lightly doped and very thin** (this constructional feature is the **key** of transistor action).

Most of the holes coming from the emitter are able to diffuse through the base region, these holes see the favourable negative potential at the collector and hence they easily reach the collector terminal to constitute the collector current, I_C. It is obvious from the above argument that the emitter current is the sum of collector current and base current.

$$I_E = I_C + I_B \qquad (I_C >> I_B)$$

Similar description can be made for a biased n-p-n transistor as shown in fig2. Here the electrons (instead of holes as in p-n-p transistor) are the majority carriers supplied by the n-type emitter region which cross the thin p-base region and are able to reach the collector to give the collector current, I_C.

Transistor Circuit configurations

Basically, there are three types of circuit connections (called configurations) for operating a transistor.

1. Common-base (CB), 2. Common-emitter (CE), 3. Common-collector (CC).

The term *common* is used to denote the electrode that is common to the input and output circuits. Because the common electrode is generally grounded, these modes of operation are frequently referred to as grounded-base, grounded-emitter and grounded-collector configurations as shown in below figure for a PNP- transistor.

Since a transistor is a 3-terminal device, one of its terminals has to be common to the input and output circuits.

CB Configuration

In this configuration, emitter current I_E is the input current and collector I_C is the output current.

The input signal is applied between the emitter and base whereas output is taken out from the collector and base as shown in below figure.

The ratio of the collector current to the emitter current is called *dc alpha* (α_{dc}) or just α of a transistor

$$\alpha_{dc} = \alpha = I_C / I_E$$

It is also called *forward current transfer ratio* ($\mathbf{h_{FB}}$). In $\mathbf{h_{FB}}$, subcript *F* stands for forward and *B* for common-base.

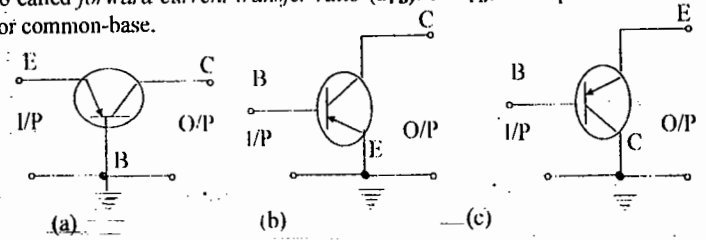


Fig.4.

The α of a transistor is a measure of the quality of a transistor; higher the value of α, better the transistor in the sense that collector current more closely equals the emitter current.

Its value ranges from 0.95 to 0.999. Obviously, it applies only to CB configuration of a transistor.

$I_C = \alpha I_E$ Now, $I_B = I_E - \alpha I_E = (1 - \alpha) I_E$ $(\because I_E = I_C + I_B)$

Incidentally, there is also an a.c. α for a transistor. It refers to the ratio of change in collector current to the change in emitter current.

$$\alpha_{dc} = \Delta I_C / \Delta I_E$$

It is also, known as *short-circuit gain* of a transistor and is written as $\mathbf{h_{fb}}$.

It may be noted that upper case subscript 'FB' indicates dc value whereas lower case subscript '*fb*' indicates ac value. For all practical purposes, $\alpha_{dc} = \alpha_{ac} = \alpha$

CE Configuration

Here, input signal is applied between the base and emitter and output signal is taken out from the collector and emitter circuit. As seen from above figure.4(b), I_B is the input current and I_C is the output current.

The ratio of the d.c. collector current to d.c base current is called *dc beta* (β_{dc}) or just β of the transistor.

$\therefore \quad \beta = I_C / I_B \quad$ or $\quad I_C = \beta I_B$

It is also called common-emitter d.c. *forward transfer ratio* and is written as h_{FE}. It is possible for β to have as high a value as 500.

While analyzing ac operation of a transistor, we use a.c β which is given by

$\beta_{ac} = \Delta I_C / \Delta I_B$.

It is also written as h_{fe}.

Relation Between α and β

$\beta = I_C/I_B$ and $\alpha = I_C/I_E \quad \therefore \beta/\alpha = I_E/I_B$

$\alpha = \beta / (1 + \beta) \quad \therefore \beta = \alpha / (1 - \alpha)$

$(1 - \alpha) = 1 / (1 + \beta)$

CC Configuration

In this case, input signal is applied between base and collector and output signal is taken out from emitter-collector circuit. Conventionally speaking, here I_B is the input current and I_E is the output current as shown in above figure.4(c). The current gain of the circuit is

$$\frac{I_E}{I_B} = \frac{I_E}{I_C} \cdot \frac{I_C}{I_B} = \frac{\beta}{\alpha} = \frac{\beta}{\beta/(1+\beta)} = (1 + \beta) = \gamma$$

Relationship Between Transistor Currents

While deriving various equations, following definitions should be kept in mind.

$$\alpha = (I_C / I_E), \quad \beta = (I_C / I_B), \quad \alpha = \frac{\beta}{1+\beta} \quad \text{and} \quad \beta = \frac{\alpha}{1-\alpha}$$

(i) $I_C = \beta I_B = \alpha I_E = \dfrac{\beta}{1+\beta} I_E$

(ii) $I_B = I_C/\beta = \dfrac{I_E}{1+\beta} = (1 - \alpha) I_E$

(iii) $I_E = I_C/\alpha = \dfrac{1+\beta}{\beta} \beta I_B = (1+\beta) I_B = \dfrac{I_B}{1-\alpha}$

(iv) The three transistor d.c. currents always bear the following relation

$$I_E : I_B : I_C :: 1 : (1-\alpha) : \alpha$$

Incidentally, it may be noted that for ac currents, small letters i_e, i_b and i_c are used.

Leakage Currents in a Transistor

***(a)* CB Configuration**

The leakage current I_{CBO} where the subscripts CBO stand for 'Collector to Base with emitter Open.' Very often, it is simply written as I_{CO}. It should be noted that

(i) I_{CBO} is exactly like the reverse saturation current I_S or I_0 of a reverse-biased diode discussed.

(ii) I_{CBO} is extremely temperature-depends because it is made up of thermally-generated minority carriers. I_{CBO} doubles for every 10° C rise in temperature for Ge and 6°C for Si

Total collector current is actually the sum of two components:

(i) current produced by normal transistor action i.e. component controlled by emitter current. Its value is a I_E and is due to majority carriers.

(ii) temperature-dependent leakage current I_{CO} due to minority carriers.

$\therefore I_C = \alpha I_E + I_{CO}$

Since $I_{CO} << I_C$ hence $\alpha \simeq I_C / I_E$

$\therefore I_C = \beta I_B + (1+\beta) I_{CO}$

CE Configuration

For a common-emitter circuit of an NPN transistor whose base lead is open. It is found that despite $I_B = 0$, there is a leakage current from collector to emitter. It is called I_{CEO}, the subscripts CEO standing for 'Collector to Emitter with base Open'.

Taking this leakage current into account, the current distribution through a *CE* circuit becomes

$I_C = \beta I_B + I_{CEO} = \beta I_B + (1 + \beta) I_{CO} = \beta I_B + I_{CO} / (1 - \alpha)$

(i) $\therefore I_C = \alpha I_B / (1-\alpha) + I_{CO} / (1-\alpha)$

Now $\beta I_B = \alpha I_E$, Substituting this value above, we get,

$I_C = \alpha I_E + I_{CEO}$

Also, $I_B = I_E - I_C$

Substituting the value of I_C from above, we have

(ii) $I_B = I_E - \alpha I_E - I_{CEO} = (1 - \alpha) I_E - I_{CEO}$

Thermal Runaway

The leakage current is extremely temperature-dependent. It almost doubles for every 10°C rise in temperature in Ge and for every 6°C rise in Si.

Any increase in I_{CO} is magnified $(1 + \beta)$ times i.e. 300 to 500 times. Even a slight increase in I_{CO} will affect I_C considerably.

As I_C increases, collector power dissipation increases which raises the operating temperature that leads to further increase in I_C.

If this succession of increases is allowed to continue, soon I_C will increase beyond safe operating value thereby damaging the transistor itself -- a condition known as *thermal runaway*.

Importance of V_{CE}

The voltage V_{CE} is very important in checking whether the transistor is
(a) defective, (b) working in cut-off
(c) in saturation or well into saturation

When $V_{CE} = V_{CC}$, the transistor is in cut-off i.e. it is turned OFF
When $V_{CE} = 0$, the transistor is in saturation i.e. it is turned fully ON.
When V_{CE} is less than zero i.e. negative, the transistor is said to be well into saturation. In practice, both these conditions are avoided.
For amplifier operation, $V_{CE} = ½ V_{CC}$.
Normal operation of a transistor lies between the above two extreme conditions of cut-off and saturation.

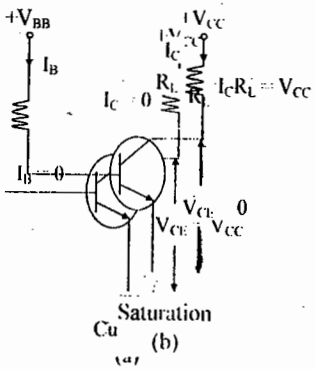


Fig.5 BJT

Operating Regions

A BJT has two junctions i.e. base-emitter and base-collector junctions either of which could be forward-biased or reverse-biased. With two junctions, there are four possible combinations of bias condition.
(i) both junctions reverse-biased.
(ii) both junctions forward-biased.
(iii) BE(Base-Emitter) junction forward-biased, BC(Base-Collector)junction reverse-biased.
(iv) BE junction reverse-biased, BC junction forward-biased.
Since condition (iv) is generally not used, we will tabulate the remaining three conditions below.

Transistor Operation Regions

BE Junction	BC Junction	Region
RB*	RB	Cut-off
FB**	FB	Saturation
FB	RB	Active

*Reverse-biased, **forward-biased

(a) Cut–off

This condition corresponds to reverse-bias for both base-emitter and base-collector junctions. In fact, both diodes act like open circuits under these conditions, which is true for an ideal transistor. In cut-off, $V_{CE} = V_{CC}$

(b) Saturation

This condition corresponds to forward-bias for both base-emitter and base-collector junctions. The transistor becomes saturated i.e. there is perfect short-circuit for both base-emitter and base-collector diodes. In this case, $V_{CE} = 0$.

(c) Active Region

This condition corresponds to forward-bias for base-emitter junction and reverse bias for base-collector junction. In this case, $V_{CE} > 0$.

BJT Switches

Very often, bipolar junction transistors are used as electronic switches. With the help of such a switch, a given load can be turned ON or OFF by a small control signal. This control signal might be the one appearing at the output of a digital logic or a microprocessor.

When using BJT as a switch, usually two levels of control signal are employed. With one level, the transistor operates in the cut-off region (open) whereas with the other level, it operates in the saturation region and acts as a short-circuit.

Typical n-p-n transistor-junction voltages at 25°C

	$V_{CE.sat}$	$V_{BE.saturation}$	$V_{BE.active}$	$V_{BE.cutin} \equiv Vr$	$V_{BE.cutoff}$
Si	0.2	0.8	0.7	0.5	0.0
Ge	0.1	0.3	0.2	0.1	-0.1

The entries in the table are appropriate for an n-p-n transistor. For a p-n-p transistor the signs of all entries should be reversed.

MAXIMUM VOLTAGE RATING

Even if the rated dissipation of transistor is not exceeded, there is an upper limit to the maximum allowable collector-junction voltage since, at high voltages, there is the possibility of voltage breakdown in the transistor.
Two types of breakdown are possible, avalanche breakdown and reach-through discussed below.

Avalanche Multiplication:

The maximum reverse-biasing voltage which may be applied before breakdown between the collector and base terminals of the transistor, under the condition that the emitter lead be open-circuited, is represented by the symbol BV_{CBO}.

Breakdown may occur because of avalanche multiplication of the current I_{CO} that crosses the collector junction.

As a result of this multiplication, the current becomes MI_{CO}, in which M is the factor by which the original current I_{CO} is multiplied by the avalance effect.

At a high enough voltage, namely, BV_{CBO}, the multiplication factor M becomes nominally infinite, and the region of breakdown is then attained. Here the current rises abruptly, and large changes in current accompany small changes in applied voltage.

The avalanche multiplication factor depends on the voltage V_{CB} between collector and base. We shall consider that

$$M \equiv \frac{1}{1-(V_{CB}/BV_{CBO})^n}$$

The parameter **n** is found to be in the range of about 2 to 10, and controls the sharpness of the onset of breakdown.

An analysis of avalanche breakdown for the CE configuration indicates that the collector-to-emitter breakdown voltage with open-circuited base, designated BV_{CEO}, is

$$BV_{CEO} = BV_{CBO}\sqrt[n]{1/h_{FE}}$$

For an n-p-n germanium transistor, a reasonable value for n, determined experimentally, is n = 6. If we now take $h_{FE} = 50$, we find that $BV_{CEO} = 0.52BV_{CBO}$.

Reach-through:

The second mechanism by which a transistor's usefulness may be terminated as the collector voltage is increased is called **punch-through, or reach-through**, and results from the increased width of the collector-junction transition region with increased collector-junction voltage (the Early effect).

As the voltage applied across the collector junction increases, the transition region penetrates deeper into the collector and base. Because neutrality of charge must be maintained, the number of uncovered charges on each side remains equal. Since the doping in the base is ordinarily substantially smaller than that of the collector, the penetration of the transition region into the base is much larger than into the collector. This process is known as **Early Effect, or Base-width Modulation**.

PARAMETERS	CB	CE	CC
1. Ri	10Ω	1 kΩ	100kΩ
2. Ro	100kΩ	10kΩ	10Ω
3. DC current gain	$\alpha = I_C/I_E$ (0.95 to 0.99)	$\beta = I_C/I_B$ (50 to 500)	$\gamma = I_E/I_B$ (51 to 501)
4. Voltage gain	Very High	Medium	≈ 1
5. Application	Radio frequency voltage amplifier	Audio frequency voltage amplifier	Buffer

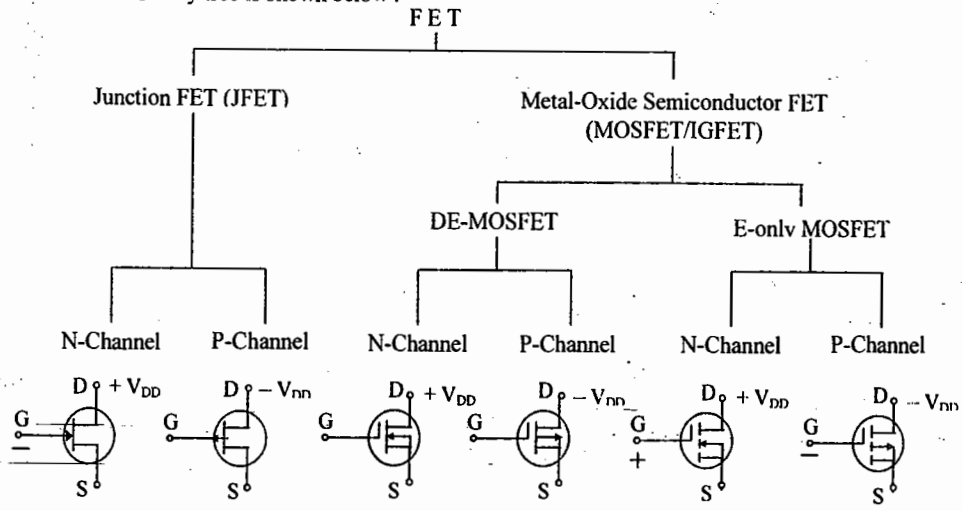
FIELD EFFECT TRANSISTORS

The acronym 'FET' stands for **field effect transistor**. It is a three-terminal unipolar solid-state device in which current is controlled by an electric field as is done in vacuum tubes.

Broadly speaking, there are two types of FETs:
(a) junction field effect transistor (JFET)
(b) metal-oxide semiconductor FET (MOSFET)

It is also called insulated-gate FET (IGFET).
It may be further subdivided into :
(i) depletion-enhancement MOSFET i.e. DE-MOSFET
(ii) enhancement-only MOSFET i.e. E-only MOSFET
Both of these can be either P-channel or N-channel devices.

The FET family tree is shown below :



Junction FET (JFET)

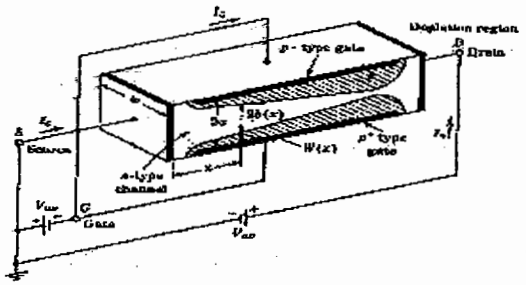
(a) Basic Construction

FET can be fabricated with either an N-channel or P-channel though N-channel is generally preferred. For fabricating an N-channel JFET, first a narrow bar of N-type semiconductor material is taken and then two P-type junctions are diffused on opposite sides of its middle part .These junctions form two P-N diodes or gates and the area between these gates is called *channel.*

The two P-regions are internally connected and a single lead is brought out which is called *gate* terminal. Ohmic contacts (direct electrical connections) are made at the two ends of the bar-one lead is called *source* terminal S and the other *drain* terminal D.

When potential difference is established between drain and source, current flows along the length of the 'bar' through the channel located between the two P-regions.

The current consists of only majority carriers which, in the present case, are electrons.



P-channel JFET is similar in construction except that it uses P-type bar and two N-type junctions. The majority carriers are holes which flow through the channel located between the two N-regions or gates.

Fig. shows, the basic structure of an n-channel field-effect transistor. The normal polarities of the drain-to-source and gate-to-source supply voltages are shown. In a p-channel FET the voltages would be reversed.

Following FET notation is worth remembering :

01. **Source.** It is the terminal through which majority carriers enter the bar. Since carriers come from it, it is called the source.

02. **Drain.** It is the terminal through which majority carriers leave the bar i.e. they are drained out from this terminal.The drain-to-source voltage V_{DS} drives the drain current I_D.

03. **Gate.** These are two internally-connected heavily-doped impurity regions which form two P-N junctions. The gate-source voltage V_{GS} reverse-biases the gates.

04. **Channel.** It is the space between two gates through which majority carriers pass from source-to- drain when V_{DS} is applied.

Schematic symbols for N-channel and P-channel JFET are shown in the above Figures. It must be kept in mind that gate arrow always points to N-type material(channel).

(b) Theory of Operation

While discussing the theory of operation of a JFET, it should be kept in mind that

1. Gates are always reversed-biased. Hence, gate current I_G is practically zero.
2. The sourced terminal is always connected to that end of the drain supply which provides the necessary charge carriers.

In an N-channel JFET, source terminal S is connected to the negative end of the drain voltage supply (for obtaining electrons).

In a P-channel JFET, S is connected to the positive end of the drain voltage supply for getting holes which flow through the channel.

Let us now consider an N-channel JFET and discuss its working when either V_{GS} or V_{DS} or both are changed.

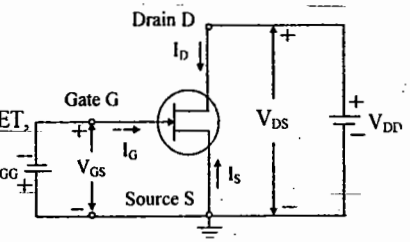


Fig.7. Circuit symbol for an n-channel FET.

(For a p-channel FET the arrow at the gate junction points in the opposite direction.) For an n-channel FET, I_D and V_{DS} are positive and V_{GS} is negative. For a p-channel FET, I_D and V_{DS} are negative and V_{GS} is positive.

(i) When $V_{GS} = 0$ and $V_{DS} = 0$

In this case, drain current $I_D = 0$, because $V_{DS} = 0$. The depletion regions around the P-N junctions are of equal thickness and symmetrical .

(ii) When $V_{GS} = 0$ and V_{DS} is increased from zero

For this purpose, the JFET is connected to the V_{DD} supply as shown in Figure. The electrons (which are the majority carriers) flow from S to D whereas conventional drain current I_D flows through the channel from D to S.

As V_{DS} is gradually increased from zero, I_D increases proportionally as per Ohm's law. It is found that for small initial values of V_{DS}, the N-type channel material acts like a resistor of constant value. It is so because V_{DS} being small, the depletion regions are not large enough to have any significant effect on channel cross-section and, hence, its resistance. Consequently, I_D increases linearly as V_{DS} is increased from zero onwards .

The ohmic relationship between V_{DS} and I_D continues till V_{DS} reaches a certain critical value called *pinch-off voltage* V_{PO} when drain current becomes constant at its maximum value called I_{DSS}.

The SS in I_{DSS} indicates that the gate is shorted to source to make sure that $V_{GS} = 0$. This current is also known as *zero-gate-voltage drain current*.
Under pinch-off conditions, separation between the depletion regions near the drain end reaches a minimum value . It should, however, be carefully noted that pinch-off does not mean 'current-off'. In fact, I_D is maximum at pinch-off.

When V_{DS} is increased beyond V_{PO}, I_D remains constant at its maximum value I_{DSS} upto a certain point. It is due to the fact that further increase in V_{DS} (beyond V_{PO}) causes more of the channel on the source end to reach the minimum width.

As more of the channel reaches the minimum width, the resistance of the channel increases at the same rate at which V_{DS} increases.
In other words, increase in V_{DS} is neutralized by increases in R_{DS}.
Consequently, $I_D = (V_{DS} / R_{DS})$ remains unchanged even though V_{DS} is increased.
Ultimately, a certain value of V_{DS} (called V_{DSO}) is reached when JFET breaks down and I_D increases to an excessive value.

(iii) When $V_{DS} = 0$ and V_{GS} is decreased from zero

In this case, as V_{GS} is made more and more negative, the gate reverse bias increases which increases the thickness of the depletion regions.
As negative value of V_{GS} is increased, a stage comes when the two depletion regions touch each other. In this condition, the channel is said to be cut-off. This value of V_{GS} which cuts off the channel and hence the drain current is called $V_{GS(off)}$.

It may be noted that $V_{GS(off)} = -V_{PO}$ or $|V_{PO}| = |V_{GS(off)}|$.

(iv) When V_{GS} is negative and V_{DS} is increased

As V_{GS} is made more and more negative, values of V_P as well as breakdown voltage are decreased.

Summary. Summarizing the above, we have that

(i) keeping V_{GS} at a fixed value (either zero or negative), as V_{DS} is increased, I_D initially increases till channel pinch-off when it becomes almost constant and finally increases excessively when JFET breaks down under high value of V_{DS}. As V_{GS} is kept fixed at progressively higher negative values, the values of V_P as well as breakdown voltage decrease.

(ii) keeping V_{DS} at a fixed value, as V_{GS} is made more and more negative, I_D decreases till it is reduced to zero for a certain value of V_{GS} called $V_{GS(off)}$.

Since gate voltage controls the drain current, JFET is called a *voltage-controlled device*.

A P-channel JFET operates exactly in the same manner as an N-channel JFET except that current carriers are holes and polarities of both V_{DD} and V_{GS} are reversed.

Since only one type of majority carrier (either electrons or holes) is used in JFETs, they are called *unipolar devices* unlike bipolar junction transistors (BJTs) which use both electrons and holes as carriers.

Static Characteristics of a JFET

We will consider the following two characteristics:

(i) Drain characteristic

It gives relation between I_D and V_{DS} for different values of V_{GS} (which is called running variable).

(ii) transfer characteristic

It gives relation between I_D and V_{GS} for different values of V_{DS}.

JFET Drain Characteristics With $V_{GS} = 0$

Such a characteristic is shown in Fig.8. and has been already discussed briefly in Art. It can be sub-divided into following four regions:

1.Ohmic Region OA

This part of the characteristic is linear indicating that for low values of V_{DS}, current varies directly with voltage following Ohm's Law. It means that JFET behaves like an ordinary resistor till point A (called knee) is reached.

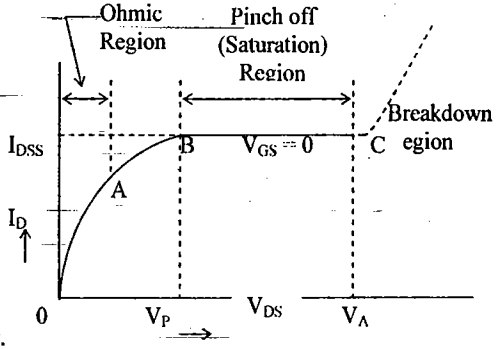


Fig.8.

2.Curve AB

In this region, I_D increases at reverse square-law rate upto point B which is called **pinch-off point**. The drain-to-source voltage V_{DS} corresponding to point B is called *pinch-off-voltage* V_P. But it essential to remember that *pinch-off* does not mean *current-off*.

3. Pinch-off Region BC

It is also known as *saturation region* or *amplified region*. Here, JFET operates as a *constant-current device* because I_D is relatively independent of V_{DS}.

It is due to the fact that as V_{DS} increases, channel resistance also increases proportionally thereby keeping I_D practically constant at I_{DSS}.

It should also be noted that the reverse bias required by the gate-channel junction is supplied entirely by the voltage drop across the channel resistance due to flow of I_{DSS} and none by external bias because $V_{GS} = 0$.

Drain current in this region is given by Shockley's equation.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

It is the normal operating region of the JFET when used as an amplifier.

4. Breakdown Region

If V_{DS} is increased beyond its value corresponding to point C (called *avalanche breakdown voltage*), JFET enters the breakdown region where I_D increases to an excessive value.

This happens because the reverse-biased gate-channel P-N junction undergoes avalanche breakdown when small change in V_{DS} produce very large changes in I_D.

It is interesting to note that increasing values of V_{DS} make a JFET behave first *as a resistor (ohmic region)*, then as a *constant-current source (pinch-off region)* and finally, as *a constant-voltage source (breakdown region)*.

Transfer Characteristic:

It is a plot of I_D versus V_{GS} for a constant value of V_{DS} and as shown in fig.9. It is similar to the transconductance characteristics of a vacuum tube or a transistor.

It is seen that when $V_{GS} = 0$, $I_D = I_{DSS}$ and when $I_D = 0$, $V_{GS} = V_P$.

The transfer characteristics approximately follows the equation.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

The above equation can be written as

$$V_{GS} = V_{GS(off)}\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

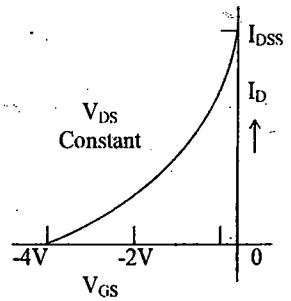


Fig.9.

This characteristics can be obtained from the drain characteristics by reading of V_{GS} and I_{DSS} values for different values of V_{DS}.

Small Signal JFET Parameters

The main parameters of a JFET when connected in common-source mode are as under:

(i) AC Drain Resistance r_d

It is the ac resistance between drain and source terminals when JFET is operating *in the pinch-off region*. It is given by

$$r_d = \frac{\text{change in } V_{DS}}{\text{change in } I_D} \text{ at } V_{GS} = \text{constant or } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at } V_{GS} = \text{constant}$$

An alternative name is *dynamic drain resistance*. It is given by the slope of the drain characteristics in the *pinch-off region*. It is sometimes written as r_{ds} emphasizing the fact that it is the resistance from drain to source.

Since r_d is usually the output resistance of a JFET, it may also be expressed as on output admittance y_{os}. Obsiously, $y_{os} = 1 / r_d$. It has a very high value.

(ii) Transconductance, g_m

It is simply the slope of transfer characteristics.

$$g_m = \frac{\text{change in } I_D}{\text{change in } V_{GS}} \text{ at } V_{DS} = \text{constant or } g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at } V_{DS} = \text{constant}$$

Its unit is Siemens (S) earlier called mho. It is also called *forward transconductance* (g_{fs}) or *forward transadmittance* y_{fs}

The transconductance measured at I_{DSS} is written as g_{mo}.

Mathematical Expression for g_m

The Shockely equation is $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$$g_m = -\frac{2I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right]$$

when $V_{GS} = 0$, $g_m = g_{mo}$ $\therefore g_{mo} = -\frac{2I_{DSS}}{V_P}$

From the above equations, we have $g_m = g_{mo}\left[1 - \frac{V_{DSS}}{V_P}\right] = g_{mo}\sqrt{\frac{I_D}{I_{DSS}}}$

(iii) Amplification Factor, μ

It is given by $\mu = \frac{\text{change in } V_{DS}}{\text{change in } V_{GS}}$ at I_D = constant or $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ at I_D = constant

It can be proved from above that

$$\mu = g_m \times r_d$$

(iv) DC Drain Resistance, R_{DS}

It is also called the static or ohmic resistance of the channel. It is given by

$$R_{DS} = V_{DS}/I_D$$

Advantages of FETs

FETs combine the many advantages of both BJTs and vacuum tubes. Some of their main advantages are:

1. high input impedance,
2. small size,
3. ruggedness,
4. long life,
5. high frequency response,
6. low noise,
7. negative temperature coefficient, hence better thermal stability,
8. high power gain,
9. a high immunity to radiations,
10. no offset voltage when used as a switch (or chopper),
11. square law characteristics.

The only *disadvantages* are :

1. small gain-bandwidth product.
2. greater susceptibility to damage in handling them.

MOSFET or IGFET

It could be further subdivided as follows:

(i) Depletion-enhancement MOSFET OR DE-MOSFET

This MOSFET is so called because it can be operated in both *depletion* mode and *enhancement* mode by changing the polarity of V_{GS}.

When negative gate-to-source voltage V_{GS} is applied, the N-channel DE-MOSFET operates in the *depletion* mode.

However, with positive gate voltage, it operates in the *enhancement* mode.

Since a channel exists between drain and source, I_D flows even when $V_{GS} = 0$.

That is why DE-MOSFET is known as **normally-ON MOSFET.**

(ii) Enhacement-only MOSFET

As its name indicates, this MOSFET operates only in the enhancement mode and has no depletion mode.

It works with *large positive gate voltages* only. It differs in construction from the DE-MOSFET in that structurally *there exists no channel between drain and source.*

Summary:

Hence, it does not conduct when $V_{GS} = 0$. That is why it is called **normally OFF** MOSFET.

In a DE-MOSFET, I_D flows even when $V_{GS} = 0$.

It operates in depletion mode with negative values of V_{GS}.

As V_{GS} is made more negative, I_D decreases till it ceases when $V_{GS} = V_{GS(off)} = V_T$ **(Threshold).**

It works in enhancement mode when V_{GS} is positive.

In the case of E-only MOSFET ,I_D flows only when V_{GS} exceeds $V_{GS} = V_T$.

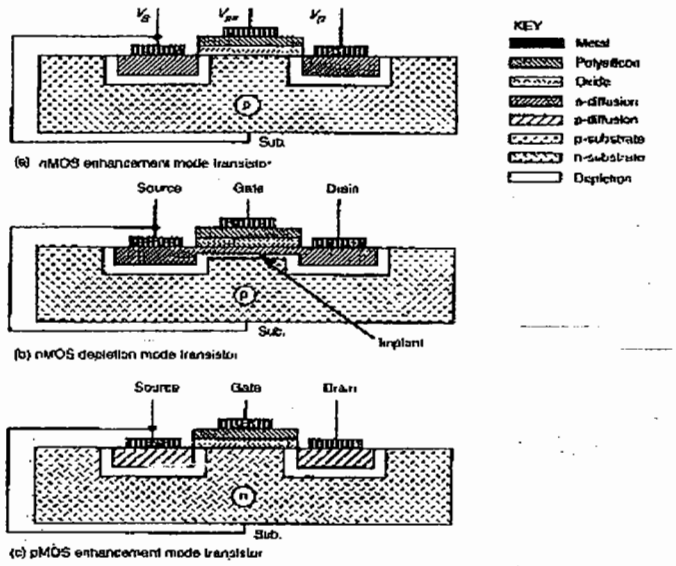


Figure 7–4 MOS transistors (V_B = 0V. Source gate and substrate to 0V)

DE-MOSFET

(a) Construction

Like JFET, it has source, gate and drain. However, as shown in aboveFigure.10., its gate is insulated from its conducting channel by an ultra-thin metal-oxide insulating film (usually of silicon dioxide SiO_2). Because of this insulating property, MOSFET is alternatively known as *insulated-gate field-effect transistor (IGFET)*. Here also, gate voltage controls drain current but main difference between JFET and MOSFET is that, in the latter case, we can apply *both positive and negative voltages to the gate because it is insulated from the channel*. Moreover, the gate, SiO_2 insulator and channel form a parallel-plate capacitor. Unlike JFET, a DE-MOSFET has only one P-region or N-region called *substrate*. Normally, substrate is shorted the source internally.

(b) working

(i) Depletion Mode of N-channel DEMOSFET

when V_{GS} = 0, electrons can flow freely from source to drain through the conducting channel which exists between them. When gate is given negative voltage, it **depletes** the N-channel of its electrons by including positive charge in it.

Greater the negative voltage on the gate, greater is the reduction in the number of electrons in the channel and, consequently, lesser its conductivity. In fact, too much negative gate voltage called $V_{GS(off)}=V_T$ can-off the channel.

For obvious reasons, negative-gate operation of a DE-MOSFET is called its depletion mode operation.

(ii) Enhancement Mode of N-channel DE-MOSFET

The circuit connections are shown in above Figure10. Again drain current flows from source to drain even with zero gate bias. When positive voltage is applied to the gate, the input gate capacitor is able to create free electrons in the channel, which increases I_D.

As positive gate voltage is increased, the number of induced electrons is increased , so conductivity of the source-to-drain channel is increased and, consequently, increasing amount of current flows between the terminals. That is why, positive gate operation of a DE-MOSFET is known as its **enhancement mode** operation.

Since gate current in both modes is negligibly small, input resistance of a MOSFET is incredibly high varying from $10^{10}\ \Omega$ to $10^{14}\Omega$. In fact, MOSFET input current is the leakage current of the capacitor unlike the input current for JFET which is the leakage current of a reverse-biased P-N junction

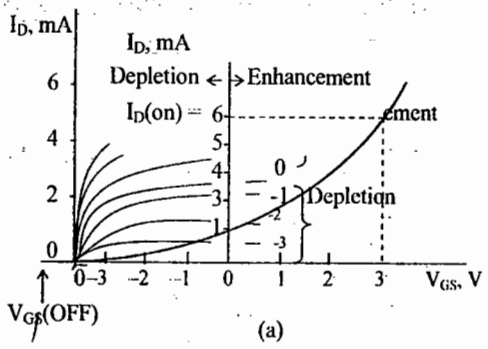


Fig.11: (a) The transfer curve (for V_{DS} = 10 V) & (b) The drain characteristics for an n-channel MOSFET which may be used in either the enhancement or the depletion mode.

Static Characteristics of a DE-MOSFET

It acts in the enhancement mode when gate is positive with respect to source and in the depletion mode when gate is negative. As usual, $V_{GS(off)}=V_T$ represents the gate-source voltage (threshold voltage) which cuts off the source-to-drain current. The transfer characteristic is shown in above Figure.11.

For a given V_{DS}, I_D flows even when V_{GS} = 0. However, keeping V_{DS} constant, as V_{GS} is made more negative, I_D keeps decreasing till it becomes zero at V_{GS} = $V_{GS(off)}$ = V_T. When used in the enhancement mode, I_D increases as V_{DS} is increased positively.

Enhancement-only N-Channel MOSFET

This N-channel MOSFET (also called NMOS) finds wide application in digital circuitry. As shown in above Figure in the NMOS, the P-type substrate extends all the way to the metal-oxide layer.

Structurally, there exists no channel between the source and drain. Hence, an NMOS can never operate with a negative gate voltage because it will induce positive charge in the space between the drain and source, which will not allow the passage of electrons between the source S and drain D.

Hence, it operates with positive gate voltages only.

With $\mathbf{V_{GS}=0}$, $\mathbf{I_D}$ is non-existent even when some positive $\mathbf{V_{DS}}$ is applied. It is found that for getting significant amount of drain current $\mathbf{I_D}$, we have to apply sufficiently high positive gate voltage $\mathbf{V_{GS}}$. This voltage is found to produce a thin layer of free electrons very close to the metal oxide film which provides channel for electrons (and hence acts like N-type inversion layer or virtual N-channel).

The minimum gate-source voltage which produces this N-type inversion layer(channel) and hence drain current is called *threshold voltage* $V_{GS(th)}=V_T$. When $V_{GS} < V_{GS(th)}(=V_T)$, I_D = 0. Drain current start only when $V_{GS} > V_{GS(th)}(=V_T)$. For a given V_{DS}, as V_{GS} is increased, virtual channel deeps and I_D increases.

A P-channel E-only MOSFET (PMOS) is constructed like NMOS except that all the P- and N-regions are interchanged. It operates with negative gate voltage V_{GS} only.

COMPARISON OF JFET AND BJT

1. FET operation depends only on the flow of majority carriers-holes for P-channel FETs and electrons for N-channel FETs. Therefore, they are called Unipolar devices. Bipolar transistor (BJT) operation depends on both minority and majority current carriers.
2. As FET has no junctions and the conduction is through an N-type or P-type semiconductor material(channel), FET is less noisy than BJT.
3. As the input circuit of FET is reverse biased, FET exhibits a much higher input impedance (in the order of 100 MΩ) and lower output impedance and there will be a high degree of isolation between input and output. So, FET can act as an excellent buffer amplifier but the BJT has low input impedance because its input circuit is forward biased.
4. FET is a voltage controlled device, i.e. voltage at the input terminal controls the output current, whereas BJT is a current controlled device, i.e. the input current controls the output current.
5. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
6. The performance of BJT is degraded by neutron radiation because of the reduction in minority- carrier lifetime, whereas FET can tolerate a much higher level of radiation since they do not rely on minority carriers for their operation.
7. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermal breakdown.
8. Since FET does not suffer from minority carrier storage effects, it has higher switching speeds and cut-off frequencies. BJT suffers from minority carrier storage effects and therefore has lower switching speed and cut-off frequencies.
9. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
10. BJTs are cheaper to produce than FETs.

APPLICATIONS OF JFET

1. FET is used as a buffer in measuring instruments, receivers since it has high input impedance and low output impedance.
2. FETs are used in RF amplifiers in FM tuners and communication equipment for the low noise level.
3. Since the input capacitance is low, FETs are used in cascade amplifiers in measuring and test equipments.
4. Since the device is voltage controlled, it is used as a voltage variable resistor in operational amplifiers and tone controls.
5. FETs are used in mixer circuits in FM and TV receivers, and communication equipment because inter modulation distortion is low.
6. It is used in oscillator circuits because frequency drift is low.

7. As the coupling capacitor is small, FETs are used in low frequency amplifiers in hearing aids and inductive transducers.
8. FETs are used in digital circuits in computers, LSD and memory circuits because of its small size.
9. As voltage-variable resistor (VVR) in operational amplifiers and tone controls etc.
10. Large-scale intergration (LSI) and computer memories because of very small size.

COMPARISON OF MOSFET WITH JFET

1. In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conducitivity of the channel.
   In the JFET the transverse electric field across the reverse biased PN junction controls the conductivity of the channel.
2. The gate leakage current in a MOSFET is of the order of 10^{-12} Amp. Hence the input resistance of a MOSFET is very high in the order of 10^{10} to 10^{15} Ω. The gate leakage current of a JFET is of the order of 10^{-9} Amp and its input resistance is of the order of 10^{8} Ω.
3. The output characteristics of the JFET are flatter than those of the MOSFET and hence, the drain resistance of a JFET (0.1 to 1 MΩ) is much higher than that of a MOSFET (1 to 50 kΩ).
4. JFETs are operated only in the depletion mode. The depletion type MOSFET may be operated in both depletiofun and enchancement mode.
5. Comparing to JFET, MOSFETs are easier to fabricate.
6. MOSFET is very susceptible to overload voltage and needs special handling during installation. It gets damaged easily if it is not properly handled.
7. MOSFET has zero offset voltage. As it is a symmetrical device, the source and drain can be interchanged. These two properties are very useful in analog signal switching.
8. Special digital CMOS circuits are available which involve near-zero power dissipation and very low voltage and current requirements. This makes them most suitable for portable systems. MOSFETs are widely used in digital VLSI circuits than JFETs because of their advantages.

COMPARISON OF N-WITH P-CHANNEL MOSFETS

1. The P-channel enhancement MOSFET is very popular because it is much easier and cheaper to produce than the N-channel device.
2. The hole mobility is nearly 2.5 times lower than the electron mobility. Thus, a P-channel MOSFET occupies a larger area than an N-channel MOSFET having the same I_D rating.
3. The drain resistance of P-channel MOSFET is three times higher than that for an identical N-channel MOSFET.
4. The N-channel MOSFET has the higher packing density which makes it faster in switching applications due to the smaller junction areas and lower inherent capacitances.
5. The N-channel MOSFET is smaller for the same complexity than P-channel device.
6. Due to the positively charged contaminants, the N-channel MOSFET may turn ON prematurely, whereas the P-channel device will not be affected.

COMPARISON OF N-WITH P-CHANNEL FETS

1. In an N-channel JFET the current carriers are electrons, whereas the current carriers are holes in a P-channel JFET.
2. Mobility of electrons is large in N-channel JFET; mobility of holes is poor in P-channel JFET.
3. The input noise is less in N-channel JFET than that of P-channel JFET.
4. The transconductance is larger in N-channel JFET than that of P-channel JFET.

SUMMARY

- The relation between Collector current amplification factor γ, Emitter current amplification factor β and Base current amplification factor α is, $\alpha = \beta / \gamma$
- Transistor is an acronym for the words **Transfer Resistor.** As the input side in forward biased and output side is reverse biased, there is transfer of resistance from a lower on input side to a higher value on the output side.
- Transistor can be used as an amplifiers, when operated in the Active Region. It is also used as a Switch, when operated in the cut-off and saturation regions.
- The three configurations of Transistor are Common Emitter, Common Base and Common Collector.
- JFET is UNIPOLAR Device (only one type of carriers either holes or electrons)
- JFET device has Higher input resistance compared to BJT and Lower input resistance compared to MOSFET.
- The disadvantage of JFET amplifier circuits is Smaller Gain – Bandwidth product compared to BJT amplifier circuits.
- $r_{ds}(ON) = \left.\frac{\partial V_{DS}}{\partial I_D}\right|_{V_{GS} = \text{constant}}$
- μ = Amplification factor $= \left.\frac{\partial V_{DS}}{\partial V_{GS}}\right|_{I_D = \text{constant}}$
- Relation between μ, r_d and g_m for a JFET is $\mu = r_d \times g_m$
- Width of the depletion region W_n for n-channel JFET, in terms of pinch off voltage V_P is $W = \left\{\frac{2\varepsilon V_p}{q N_D}\right\}^{1/2}$
- Expression for I_{DS} in terms of I_{DSS}, V_{GS} and V_P is $I_D = I_{DSS}\left\{1 - \frac{V_{GS}}{V_P}\right\}^2$
- I_{DSS} = Saturation valu8e of Drain current when gate is shorted to source.
- For zero drift current, in the case of JFETs, $|V_p| - |V_{GS}| = 0.623V$

OBJECTIVE - 1

1. For identical construction, ... types of bipolar junction transistors (BJTs) have faster switching times.
2. Expression for I_{CEO} in terms of I_{CBO} and α is .....
3. β' of a BJT is defined as .....
4. β' of a transistor (BJT) is .....
5. Relation between β' and β is .....
6. β' is synonymous to ..... and β is same as .....
7. β is ..... (for DC Currents).
8. β' is ..... (for AC Currents).
9. In a BJT the arrow on the emitter lead specifies the direction of ..... where the emitter-base junction is ..... biased.
10. IGFET is the other name for ..... device.
11. In JFET recombination noise is less because it is ..... device.
12. The disadvantage of JFET amplifier circuit is .....
13. The D, G, S terminals of JFET are similar to .....Terminals of BJT respectively.
14. The voltage V_{DS} at which I_D tends to level off, in JFET is called .....
15. The voltage V_{GS} at which I_D becomes zero in the transfer characteristic of JFET is called .....
16. JFET can be used as ..... resistor.
17. The square law device is .....
18. The MOSFET that can be used in both enhancement mode and depletion mode is ..... .
19. The operation of a FET depends upon the flow of .... carriers only. It is therefore a ..... device.
20. The break down voltage of a transistor with its base open is BV_{CEO} and with emitter open is BV_{CBO}, then
    (A) B V_{CEO} = B V_{CBO}
    (B) B V_{CEO} > B V_{CBO}
    (C) B V_{CEO} < B V_{CBO}
    (D) is not related to B V_{CBO}
21. DIn a bipolar transistor at room temperature, if the emitter current is doubled, the voltage across its base-emitter junction.
    (A) Doubles (B) halves
    (C) Increases by about 20 mv
    (D) decrease by about 20v
22. The early-effect in bipolar transistor is caused by
    (A) Fast turn-on (B) fast turn-off
    (C) large collector-base reverse
    (D) large emitter-base forward bias
23. Base-to-emitter voltage V_{BE} in a forward biased transistor decreases with increase of temperature at the following rate :
    (A) 25 mv/deg c (B) 0.25 mv/deg c
    (C) 2.5 mv/deg c (D) 0.6 mv/deg c
24. If a transistor is operating with both of its junctions forward biased, but with the collector-base forward bias greater than the emitter-base forward bias, then it is operating in the
    (A) forward active mode
    (B) reverse saturation mode
    (C) reverse active mode
    (D) forward saturation mode
25. In a bipolar transistor at room temperature, if the emitter current is doubled, the voltage across its base-emitter junction
    (A) doubles
    (B) halves
    (C) increases by about 20 mV
    (D) decreases by about 20 m V

26. In a transistor having finite β, the forward bias across the base-emitter junction is kept constant and the reverse bias across the collector-base junction is increased. Neglecting the leakage across the collector-base junction and the depletion generation current, the base current will
(A) increase (B) decrease
(C) remain constant (D) none.

27. An n-channel JFET has a pinch-off voltage of $V_P = -5V$, $V_{DS}(max) = 20$ V, and $g_m = 2$ mA / V. The minimum 'ON' resistance is achieved in the JFET for
(A) $V_{GS} = -7V$ and $V_{DS} = 0$ V
(B) $V_{GS} = 0$ V and $V_{DS} = 0$ V
(C) $V_{GS} = 0$ V and $V_{DS} = 20$ V
(D) $V_{GS} = -7V$ and $V_{DS} = 20$ V

28. Consider the following four common type of transistors.
1. Point Contact Tansistor
2. Bipolar Junction Transistor
3. MOS Field Effect Transistor
4. Junction Field Effect Transistor

The correct arrangement of these transistors in the increasing order of input impedance is
(A) 1, 2, 4, 3 (B) 1, 2, 3, 4
(C) 2, 1, 3, 4 (D) 2, 1, 4, 3

29. In a transistor amplifier, the reverse saturation current I_{CO}
(A) doubles for every 10° C rise in temperature
(B) doubles for every 1° C rise in temperature
(C) increases linearly with temperature
(D) doubles for every 5° C rise in temperature

30. If $\alpha = 0.981$, $I_{CO} = 6\ \mu A$ and $I_R = 100\ \mu A$ for a transistor, then the value of I_C will be
(A) 2.3 mA (B) 3.1
(C) 4.6 mA (D) 5.2 mA

31. In a transistor having finite B, the forward bias across the base emitter junction is kept constant and the reverse bias across the collector-base junction is increased. Neglecting the leakage across the collector-base junction and the depletion region generation current, the base current will
(A) increase (B) decrease
(C) remain constant (D)none

32. The threshold voltage of an n-channel MOSFET can be increased by
(A) increasing the channel dopant concentration
(B) reducing the channel dopant concentration
(C) reducing the gate oxide thickness
(D) reducing the channel length

33. Match each of the items A, B and C with and appropriate item from 1, 2, 3, 4 and 5.
(A) The current gain of a BJT will be increased if
(B) The current gain of a BJT will be reduced if
(C) The break-down voltage of a BJT will be reduced if

1. The collector doping concentration is increased
2. The base width is reduce
3. The emitter doping concentration to base doping concentration ratio is reduced
4. The base doping concentration is increased keeping the ratio of the emitter doping concentration to base doping concentration constant
5. The collector doping concentration is reduced

(A) A – 2, B – 3, C – 1
(B) A – 2, B – 1, C – 3
(C) A – 3, B – 1, C – 2
(D) A – 1, B – 2, C – 3

34. The Ebers-Moll model is applicable to
(A) bipolar junction transistors
(B) NMOS transistors
(C) unipolar junction transistors
(D) junction field-effect transistors

35. Match each of the items A, B and C with and appropriate item from 1, 2, 3, 4 and 5

List – I
(A) Common – collector amplifier
(B) Common – emitter amplifier
(C) Common – base amplifier

List - II
1. Provides voltage gain but no current gain
2. Provides current gain but no voltage gain
3. Provides neither voltage nor power gain
4. Provides neither current nor power gain
5. Provides both voltage and current gain

(a) A – 5, B – 3, C – 1
(b) A – 2, B – 5, C – 2
(c) A – 4, B – 1, C – 2
(d) A – 2, B – 5, C – 1

Answers

01. NPN 02. $I_{CEO} = I_{CBO}/(1 - \alpha)$

03. $\beta = \left.\frac{\partial I_C}{\partial I_B}\right|_{V_{CE}} = \text{constant}$

04. Small Signal Common Emitter Forward Current Gain

05. $\beta' = \frac{\beta}{\left[1 - (I_{CB0} + I_B)\frac{\partial h_{FE}}{\partial I_C}\right]}$

07. Large Signal Current Gain

08. Small Signal Current Gain

09. Hole or conventional current, forward

10. MOSFET 11. UNIPOLAR

12. gain band width product is less.

13. C, B, E 14. Pinch off Voltage

15. Pinch off Voltage 16. voltage variable

17. JFET

18. Depletion MOSFET (DMOSFET)

19. Majority, Unipolar

20.C 21.B 22.C 23.C 24.B 25.B

26.B 27.C 28.D 29.A 30.D

31.B 32.B 33.A 34.A

35.D

OBJECTIVE - 2

01. The early effect in a bipolar junction transistor is caused by
(A) fast turn – on
(B) fast turn – off
(C) large collector – base reverse bias
(D) large emitter – base forward bias

02. The widths of the base in a GaAs transistor and in a Si transistor (both n – p – n type) are equal. GaAs transistor works at higher frequency
(A) the band gap of GaAs is higher than that of Si
(B) the base transit time is lower in GaAs.
(C) the negative differential mobility in GaAs favours operational very high frequency
(D) Si transistor works at higher frequency compared to GaAs transistor.

03. Which one of the following is the exact expression for I_{CEO} (i.e., collector to emitter current with base open) in a junction transistor?
(A) $\alpha.I_{CBO}$ (B) $\frac{\alpha}{1-\alpha}.I_{CBO}$
(C) $\frac{I_{CBO}}{1-\alpha}$ (D) $(1-\alpha)\,I_{CBO}$

04. If for a silicon n-p-n transistor, the base-to- emitter voltage (V_{BE}) is 0.7V and the collector-to-base voltage (V_{CB}) is 0.2V, then the transistor operating in the
(A) normal active mode
(B) saturation mode
(C) inverse active mode
(D) cut off mode

05. How can the channel width in a junction field effect transistor be controlled?
(A) By two back-biased p-n junctions
(B) By the length of the source
(C) By the length of the drain
(D) By the length of both the source and the drain

06. The voltage gain of a given common source JEFT amplifier depends on its
(A) input impedance
(B) amplification factor
(C) dynamic drain resistance
(D) drain load resistance

07. The set of transistor characteristics that enables α to be directly determined from the slope is
(a) The common emitter output characteristics
(b) The common emitter transfer characteristics
(c) The common base input characteristics
(d) The common base transfer characteristics

08. The effective channel length of a MOSFET in saturation decreases with increase in
(a) gate voltage
(b)drain voltage
(c) source voltage
(d) body voltage

09. The internal resistance of a current source used in the model of a BJT while analyzing a circuit using BJT is
(a) Very high
(b) Very low
(c) Zero
(d) Of the order of a few mega-ohms

10 In a transistor, the forward bias across the base emitter junction is kept constant and the reverse bias across the collector base junction is increased. Neglecting the leakage across the collector . base junction and the depletion region generation current. The base current will
(a) increase
(b) decrease
(c) remain constant
(d) none of these

11.In a common emitter amplifier. the un bypassed emitter resistance provides
(a) voltage shunt feedback
(b) current series feedback
(c) negative voltage feedback
(d) positive current feedback

12. α-cut off frequency of a bipolar junction transistor
(a) increase with the increase in base width.
(b) increase with increase in the collector width.
(c) increase with the increase in temperature.
(d) increase with decrease in the base width.

13. The breakdown voltage of a transistor with its base open is BV_{CEO} and that with the emitter open is BV_{CBO} then
(a) $BV_{CEO} = BV_{CBO}$
(b) $BV_{CEO} > BV_{CBO}$
(c) $BV_{CEO} < BV_{CBO}$
(d) BV_{CEO} is not related to BV_{CEO}

14. Two identical FETs, each by characterized by the parameters g_m and r_d are connected in parallel. The composite FET is then characterized by the parameters
(a) $g_m/2$ and $2r_d$ (b) $g_m/2$ and $r_d/2$
(c) $2g_m$ and $r_d/2$ (d) $2g_m$ and $2r_d$

15 Thermal runaway in a transistor biased in the active region is due to
(a) heating of the transistor
(b) changes in β which increases with temperature
(c) base emitter voltage V_{BE} which decreases with rise in temperature
(d) Change in reverse collector saturation current due to rise in temperature

16 In a transistor amplifier, the reverse saturation current I_0 is.
(a) doubled for every 10^0C rise in temperature
(b) doubled for every 1^0 C rise in temperature
(c) increased linearly with temperature
(d) doubled for every 5^0 C rise in temperature

17. If a transistor is operation with both of its junctions forward biased, but with the collector base forward bias greater than the emitter base forward bias than, it is operating in the
(a) forward active mode
(b) reverse saturation mode
(c) reverse active mode
(d) forward saturation mode

18.The common emitter short circuit current gain β of a transistor
(a) is monotonically increasing function of the collector current I_c'
(b) is a monotonically decreasing function of I_c.
(c) Increases with I_c' for low I_c reaches a maximum and then decreases with further increases in I_c'
(d) is a not function of I_c'

19. The 'Pinch-off" voltage of a JFET is 5 V. Its "Cut-off" voltage is
(a) $(5.0)^{1/2}$V (b) 2.5 V
(c) 5.0 V (d) $(5.0)^{3/2}$ V

20 Which of the following effects can be caused by a rise in temperature?
(a) Increase in MOSFET Current (IDS)
(b) Increase in BJT current (Ic)
(c) Decreases in MOSFET Current (IDS)
(d) Decreases in BJT current (Ic)

21. Consider the following statements:
1. The β of a bipolar transistor reduces if base width is increased
2. The β of a bipolar transistor increases if the doping concentration in the base is increased
Which one of the following is correct?
(a) 1 is FALSE and 2 is TRUE
(b) Both 1 and 2 are TRUE.
(c) Both 1 and 2 are FALSE
(d) 1 isTRUE and 2 is FALSE

22. Which one of the following statements is correct in respect of BJT?
(a) Avalanche multiplication starts when the reverse biased collector-base voltage V_{CB} equals the avalanche breakdown voltage BV_{CBO}
(b) The early effect starts as soon as punch-through occurs in a transistor.
(c) The small signal current gain h_{fe} = large signal current gain h_{FE} when $\partial h_{FE}/\partial I_c = 0$.
(d) In the CE mode, a transistor can be cut off by reducing I_B to zero.

23. The gain of a bipolar transistor drops at high frequencies. This is because of the
(a) Coupling and bypass capacitors.
(b) Early effect.
(c) Inter-electrode transistor capacitances.
(d) Coupling and bypass capacitors, and inter-electrode transistor capacitances.

24. When the gate-to-source voltage(V_{GS}) of a MOSFET with threshold voltage of 400 mV, working in saturation is 900 mV, the drain current is observed to be 1 mA. Neglecting the channel width modulation effect and assuming that the MOSFET is operating at saturation, the drain current for an applied V_{GS} of 1400 mV is
(a) 0.5 mA (b) 2.0 mA
(c) 3.5 mA (d) 4.0 mA

25. Match List – I (Device) with List-II (Associated Term) and select the correct answer using the code given below the lists:

List-I	List –II
A. Diode	1. Pinch – off voltage
B. S.C.R	2. Holding current
C. B.J.T	3. Forward resistance
D. F.E.T	4. Active region

	A	B	C	D
(a)	3	4	2	1
(b)	1	2	4	3
(c)	3	2	4	1
(d)	1	4	2	3

26. A bipolar junction transistor is in saturation region. Given Vcc = 10 V, RC = 1 kΩ, h_{FE} = 100 and V_{CEsat} = 0.3 V. What is the collector current in saturation?
(a) 10 mA (b) 9.7 mA
(c) 0 mA (d) 1 mA

27. An emitter in a bipolar junction transistor is doped much more heavily than the base as it increases the
(a) emitter efficiency
(b) base transport factor
(c) forward current gain
(d) all the three given above

28. Match List- I (Devices) with List-II (Characteristic) and select the correct answer using the code given below the lists.

List-I	List- II
A. BJT	1. Volatage controlled negative resistance
B. MOSFET	2. High current gain
C. Tunnel diode	3. Voltage regulation
D. Zener diode	4. High input Impedance

	A	B	C	D
(a)	1	4	2	3
(b)	2	4	1	3
(c)	2	3	1	4
(d)	1	3	2	4

29. A junction transistor operating at room temperature with I_c = 2mA; where KT /q = 25mV has β = 100. The value of parameters g_m in Mhos and r_s in ohms will be respectively
(a) 0.04 and 2500 (b) 0.08 and 1250
(c) 0.5 and 800 (d) 0.08 and 5000

30. In n- channel JFET has a pinch – off voltage of V_0 = -5V , V_{DS}(max) = 20V and g_m =20mA/V .The minimum 'ON' resistance is achieved in the JFET for
(a) V_{GS} = -7V and V_{DS} =0V
(b) V_{GS} = 0V and V_{DS} =0V
(c) V_{GS} = 0V and V_{DS} =20V
(d) V_{GS} = -7V and V_{DS} =20V

31. If α = 0.995, I_E = 10mA and Ico = 0.5μA, then I_{CEO} will be
(a) 25 μA (b) 100μA
(c) 10.1μA (d) 10.5 μA

32. If an amplifier with gain of 1000 and feedback of β = - 0.1 had a gain change of 20% due to temperature, the change in gain of the feedback amplifier would be
(a) 10% (b) 5%
(c) 0.2% (d) 0.01 %

33. If α = 0.98, I_{co}= 6 μA and I_B =100 μA for a transistor, then the value of I_c will be
(a) 2.3 mA (b) 3.1 mA
(c) 4.6 mA (d) 5.2 mA

34. For a PNP transistor, α = α_R = 0.9 and I_{co}= 10 μA, the value of I_{CS} will be
(a) 15.2μA (b) 52.6 μA
(c) 72.5 μA (d) 1.2 μA

35. A Si transistor has a thermal ratings, T_{max} = 150°C and Q_{ic} = 0.7 °C/W . The power which transistor could dissipate if the case could be maintained at 50°C is
(a) 143W (b) 59W
(c)110W (d)85W

36. In a transistor h_{fe} =50, h_{ie} =830Ω, h_{oe} =10^{-4} . Its out put resistance when used in CB configuration is about
(a) 2MΩ (b) 700KΩ
(c) 2.5MΩ (d) None

KEYS:

01.c	02. b	03.c	04.a	05.a	06. b
07.d	08.b	09.a	10.b	11.b	12.b
13.c	14.c	15.d	16.a	17.b	18.c
19.c	20.b	21.d	22.a	23.c	24.d
25.c	26.b	27.c	28.b	29.b	30.c
31.b	32.c	33.d	34.b	35.b	36.d

PREVIOUS IES QUESTIONS:

01. A transistor with emitter base voltage (V_{EB}) of 20mV has a collector current (I_C) of 5mA. For V_{EB} of 30mV, I_C is 30mA. If V_{EB} is 40mV, then the I_C will be
(a) 55mA (b) 160mA
(c) 180mA (d) 270mA

02. Match **List-I** (Devices) with **List-II**(characteristics) and select the correct answer using the codes given below the lists:

List-I
A. BJT
B. MOSFET
C. Tunnel diode
D. Zener diode

List-II
1. Voltage controlled –ve resistance
2. High current gain
3. Voltage regulation
4. High input impedence

Codes:

	A	B	C	D
(a)	1	4	2	3
(b)	2	4	1	3
(c)	2	3	1	4
(d)	1	3	2	4

03. In a junction transistor, the collector cutoff current 'I_{CBO}' reduces considerably by doping the
(a) emitter with high level of impurity
(b) emitter with low level of impurity
(c) collector with high level of impurity
(d) collector with low level of impurity

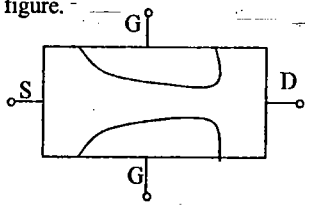
04. In a junction transistor biased for operation at emitter current 'I_E' and collector current 'I_C' the transconductance 'g_m' is
(a) kT/qI_E (b) qI_E/kT
(c) I_C/I_E (d) I_E/I_C

05. To avoid thermal runway in the design of an analog circuit, the operating point of the BJT should be such that it satisfies the condition
(a) $V_{CE} = V_{CC}/2$ (b) $V_{CE} \le V_{CC}/2$
(c) $V_{CE} > V_{CC}/2$ (d) $V_{CE} \le 0.78\ V_{CC}$

06. Consider the following devices:
1. BJT in CB mode
2. BJT in CE mode
3. JFET
4. MOSFET
The correct sequence of these devices in increasing order of their input impedance is
(a) 1, 2, 3, 4 (b) 2, 1, 3, 4
(c) 2, 1, 4, 3 (d) 1, 3, 2, 4

07. **Assertion(A):** FETs are more suitable at the input stages of millivoltmeter and CROs than BJTs.
Reason(R): A FET has lower output impedance than a BJT.
(a) Both A and R are true and R is the correct explanation of A.
(b) Both A and R are true but R is NOT the correct explanation of A.
(c) A is true but R is false.
(d) A is false but R is true.

08. In a biased JFET, the shape of the channel is an shown in the given figure.



because
(a) it is the property of the material used
(b) the drain end is more reverse biased than source end.
(c) the drain end is more forward biased than source end
(d) the impurity profile varies with the distance from source

09. A transistor has a current again of 0.99 in the CB mode. Its current gain in the CC mode is
(a) 100 (b) 99 (c) 1.01 (d) 0.99

10. Match **List-I** (Biasing of the junctions) with **List-II** (Functions) and select the correct answer using the codes given below the lists:

List-I
A. E-B junction forward bias and C-B junction reverse bias
B. Both E-B and C-B junctions forward bias
C. E-B junction reverse bias and C-B junction forward bias
D. Both E-B and C-B junctions reverse bias

List-II
1. Very low gain amplifier
2. Saturation C-B junctions
3. High gain and amplifier
4. Cut-off condition

Codes:

	A	B	C	D
(a)	2	3	1	4
(b)	3	2	1	4
(c)	3	2	4	1
(d)	2	3	4	1

11. Match **List-I** (Structures / characteristics) with **List-II** (Reasons) in respect of JFET and select the correct answer using the codes given below the lists:

List-I
A. n-channel JFET is better than p-channel JFET
B. Channel is wedge shaped
C. Channel is not completely closed at pinch-off
D. Input impedance is high

List-II
1. Reverse bias increases along the channel
2. High electric field near the drain and directed towards source
3. Low leakage current at the gate terminal
4. Better frequency performance since terminal $\mu_0 >> \mu_p$

Codes:

	A	B	C	D
(a)	4	1	2	3
(b)	4	2	1	3
(c)	3	1	2	4
(d)	3	2	1	4

12. The output current versus input voltage transfer characteristic of an n-channel JFET in such that there is
(a) zero current flow at zero input voltage bias
(b) current flow only when a positive input threshold voltage is crossed.
(c) current flow only when a negative input cut – off voltage bias is crossed.
(d) no cut – off input voltage.

13. In a MOS transistor, the gate source input impedance is
1. lower than the impedance of a BJT
2. higher than the input impedance of a BJT
3. lower than the input impedance of a JFET.
4. higher than the input impedance of a JFET.
(a) 1 alone (b) 2 and 3
(c) 4 alone (d) 2 and 4

14. At 25^0C, the collector – emitter voltage drop of a silicon transistor at saturation is approximately
(a) 0.1 V (b) 0.3 V (c) 0.5 V (d) 0.7 V

15. **Assertion (A):** The semiconductor devices like BJTs have a maximum temperature of operation, beyond which they do no function.
Reason(R): Extrinsic, p-type and n-type semiconductors behave as intrinsic beyond that temperature and the effect of doping is lost.
(a) Both A and R are true and R is the correct explanation of A.
(b) Both A and R are true but R is NOT the correct explanation of A.
(c) A is true but R is false.
(d) A is false but R is true.

16. **Assertion (A):** A bipolar junction transistor has high gain, high emitter efficiency and high speed.
Reason(R): The transistor has heavy emitter doping and narrow base width.
(a) Both A and R are true and R is the correct explanation of A.
(b) Both A and R are true but R is NOT the correct explanation of A.
(c) A is true but R is false.
(d) A is false but R is true.

17. Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I
A. Gunn Diode
B. Solar Cell
C. MOSFET
D. SCR

List-II
1. Junction less device
2. Single junction device
3. double junction device
4. Triple junction device

Codes:

	A	B	C	D
(a)	1	2	3	4
(b)	3	4	1	2
(c)	1	4	3	2
(d)	3	2	1	4

18. A bipolar junction transistor has a common base forward short circuit current gain of 0.99. Its common emitter forward short circuit current gain will be
(a) 50 (b) 99
(c) 100 (d) 200

19. **Assertion (A):** In a transistor the thickness of the base region is kept as small as possible.
Reason(R): By keeping the base thickness small, a large electric field is produced between the emitter and the collector which makes the transistor fast-acting.
(a) Both A and R are true and R is the correct explanation of A.
(b) Both A and R are true but R is NOT the correct explanation of A.
(c) A is true but R is false.
(d) A is false but R is true.

20. Match **List-I** (Equation) with **List-II** (Relation between/Description) and select the correct answer using the codes given below the lists.

List-I
A. Continuity equation
B. Einstein's equation
C. Poisson's equation
D. Diffusion equation

List-II
1. Relates diffusion constant with mobility
2. Relates charge density with electric field
3. Relates flow with rate of change of concentration in space.
4. Rate of change of minority carrier density with time

Codes:

	A	B	C	D
(a)	4	1	3	2
(b)	4	1	2	3
(c)	1	4	2	3
(d)	1	4	3	2

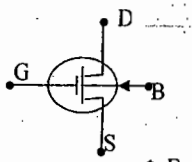
21. How can the channel width in a junction field effect transistor be controlled?
(a) By two back-biased p-n junctions
(b) By the length of the source
(c) By the length of the drain
(d) By the length of both the source and the drain

22. Which one of the following is the correct relation ship between the band gap of a material used in a photo detector and the energy of the incident photon?
(a) $E_g > hc/\lambda$ (b) $h\upsilon^2/\lambda > E_g$
(c) $h\upsilon > E_g$ (d) $1/2h\upsilon \le E_g$

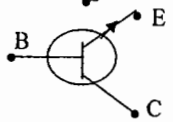
23. Match **List-I** (Semiconductor Device) with **List-II** (Symbol Used) and select the correct answer using the codes given below the lists:

List-I
List-II

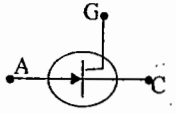
A. n-p-n transistor



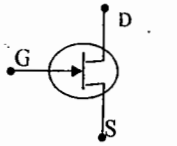
B. SCR



C. FET



D. MOSFET



Codes:

	A	B	C	D
(a)	2	3	4	1
(b)	4	1	2	3
(c)	2	1	4	3
(d)	4	3	2	1

24. Which one of the following is the exact expression for I_{CEO} (i.e. collector to emitter current with base open) in a junction transistor?

(a) $\alpha . I_{CBO}$ (b) $\frac{\alpha}{1-\alpha} . I_{CBO}$
(c) $\frac{I_{CBO}}{1-\alpha}$ (d) $(1-\alpha)I_{CBO}$

(where I_{CBO} is the collector to base current with emitter open, and α is the common base current gain)

25. Consider the following statements:
FETs when compared to BJTs have
1. high input impedance
2. current flow due to majority carriers
3. low input impedance
4. current flow due to minority carriers
Which of the statements given above are correct?
(a) 1 and 4 (b) 2 and 3
(c) 3 and 4 (d) 1 and 2

26. How is an N – channel Junction Field Effect Transistor operated as an amplifier?
(a) With a forward bias gate – source junction
(b) With a reverse bias gate – source junction
(c) With an open gate – source junction
(d) With a shorted gate – source junction

27. For a npn bipolar transistor, what is the main stream of current in the base region?.
(a) Drift of holes
(b) diffusion of holes
(c) Drift of electrons
(d) Diffusion of electrons

28. What is the most noticeable effect of a small increase in temperature in the common emitter connected BJT?
(a) Increase in I_{CBO}
(b) Increase in output resistance
(c) Decrease in forward current gain
(d) Increase in forward current gain.

29. For BJT, early voltage V_A is 100 V. In common emitter configuration, quiescent V_{CE} is 10 V. What percentage change in quiescent I_C would occur, if early voltage V_A is made ∞?
(a) 10 % (b) 20%
(c) 5 % (d) 0%

30. While using a bipolar junction transistor as an amplifier, the collector and emitter terminals got interchanged mistakenly. Assuming that the amplifier is a common emitter amplifier and the biasing is suitably adjusted, the interchange of terminals will result into which one of the following?
(a) Zero gain
(b) Infinite gain
(c) Reduced gain
(d) No change in gain at all

31. In n – channel enhancement MOSFET at a fixed drain voltage
(a) the drain current is maximum at zero gate voltage and it decreases with applied negative gate voltage
(b) the drain current has a finite values at zero gate voltage and it increases or decreases with the applied voltage of proper polarity
(c) the drain current is zero at zero gate voltage and it increases with the positive applied gate voltage
(d) the drain current is zero for negative bias voltage to gate and it increases as the negative gate bias is decreased in magnitude

32. The data sheet for a certain JFET (Junction Field Effect Transistor) indicates that I_{DSS} (drain to source current with gate shorted) = 15 mA and V_{GS} (off) (Cut - off value of gate to source voltage) = - 5V. What is the drain current for V_{GS} - 2 V?
(a) 58. 8 mA (b) 29.4 mA
(c) 9.6 mA (d) 5.4 mA

KEY:

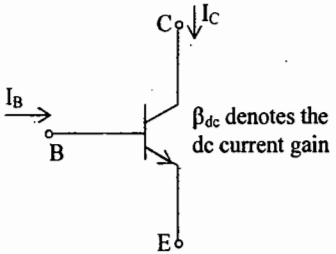
1.a	2.b	3.a	4.b	5.b	6.a
7.a	8.b	9.a	10.b	11.a	12.c
13.d	14.b	15.a	16.a	17.a	18.b
19.c	20.b	21.a	22.c	23.a	24.c
25.d	26.d	27.d	28.a	29.c	30.c
31.c	32.d				

PREVIOUS GATE QUESTIONS:

1. The Early effect in a bipolar junction transistor is caused by **GATE - 1999**
(a) fast turn-on
(b) fast turn-off
(c) large collector-base reverse bias
(d) large emitter-base forward bias

2. MOSFET can be used as a **GATE - 2001**
(a) current controlled capacitor
(b) voltage controlled capacitor
(c) current controlled inductor
(d) voltage controlled inductor

3. If the transistor in the figure is in saturation, then **GATE - 2002**



(a) I_C is always equal to $\beta_{dc}I_B$
(b) I_C is always equal to $-\beta_{dc}I_B$
(c) I_C is greater than or equal to $\beta_{dc}I_B$
(d) I_C is less than or equal to $\beta_{dc}I_B$

4. For an n-channel enhancement type MOSFET, if the source is connected at a higher potential than that of the bulk(i.e. $V_{SB}>0$), the threshold voltage V_T of the MOSFET will **GATE - 2003**
(a) remain unchanged
(b) decrease
(c) Change polarity
(d) increase

5. The impurity commonly used for realizing the base region of a silicon n-p-n transistor is **GATE - 2004**
(a) Gallium (b) Indium
(c) Boron (d) Phosphorus

6. If for a silicon n-p-n transistor, the base-to-emitter voltage (V_{BE}) is 0.7 V and the collector-to-base voltage (V_{CB}) is 0.2V, then transistor is operating in the **GATE – 2004**
(a) normal active mode
(b) saturation mode
(c) inverse active mode
(d) cutoff mode

7. Consider the following statements S1 and S2.
S1: The β of a bipolar transistor reduces if the base width is increased.
S2: The β bipolar transistor increases If the doping concentration in the base is increased.
Which one of the following is correct? **GATE - 2004**
(a) S1 is FALSE and S2 is TRUE
(b) Both S1 and S2 are TRUE
(c) Both S1 and S2 are FALSE
(d) S1 is TRUE and S2 is FALSE

8. The phenomenon known as "Early Effect" in a bipolar transistor refers to a reduction of the effective base-width caused by. **GATE - 2006**
(a) electron-hole recombination at the base
(b) the reverse biasing of the base-collector junction
(c) the forward biasing of emitter-base junction
(d) the early removal of stored base charge during saturation-to-cutoff switching.

9. An n-channel JEFT has I_{DSS} = 2mA and V_P = -4V. Its transconductance g_m (in mA/V) for an applied gate to source voltage V_{GS} of –2V is
GATE - 1999
(a) 0.25 (b) 0.5
(c) 0.75 (d) 1.0

10. When the gate-to-source voltage (V_{GS}) of a MOSFET with threshold voltage of 400 mV, working in saturation is 900 mV, the drain current is observed to be 1 mA. Neglecting the channel width modulation effect and assuming that the MOSFET is operating at saturation, the drain current for an applied V_{GS} of 1400 mV is
GATE – 2003
(a) 0.5 mA (b) 2.0 Ma
(c) 3.5 mA (d) 4.0 mA

11. Consider the following statements S1 and S2.
S1: The threshold voltage (V_T) of a MOS capacitor decreases with increase in gate oxide thickness
S2: The threshold voltage (V_T) of a MOS capacitor decreases with increase in substrate doping concentration
GATE - 2004
(a) S1 is FALSE and S2 is TRUE
(b) Both S1 and S2 are TRUE
(c) Both S1 and S2 are FALSE
(d) S1 is TRUE and S2 is FALSE

12. The drain of an n-channel MOSFET is shorted to the gate so that V_{GS} = V_{DS}. The threshold voltage (V_T) of MOSFET is 1 V. If the drain current (I_D) is 1 mA for V_{GS} = 2V, then for V_{GS} = 3V, I_D is
GATE – 2004
(a) 2 mA (b) 3 mA
(c) 9 mA (d) 4 mA

13. The neutral base width of a bipolar transistor, biased in the active region, is 0.5 μm. The maximum electron concentration and the diffusion constant in the base are $10^{14}/cm^3$ and D_n = 25 cm^2/sec respectively. Assuming negligible recombination in the base, the collector current density is (the electron charge is 1.6 x 10^{-19} Coulomb) **GATE – 2004**
(a) 800 A/cm^2 (b) 8 A/cm^2
(c) 200 A/cm^2 (d) 2 A/cm^2

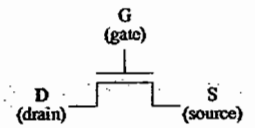
14. A MOS capacitor made using p type substrate is in the accumulation mode. The dominant charge in the channel is due to the presence of **GATE – 2005**
(a) holes
(b) electrons
(c) positively charged ions
(d) negatively charged ions

15. Consider the following two statements about the internal conditions in an n-channel MOSFET operating in the active region
S1: The inversion charge decreases from source to drain.
S2: The channel potential increases from source to drain
Which of the following is correct?
a) Only S2 is true
b) Both S1 and S2 are false
c) Both S1 and S2 are true, but S2 is not a reason for S1
d) Both S1 and S2 are true, and S2 is a reason for S1:

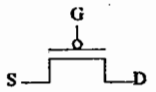
KEY:

1.c	2.b	3.d	4.d	5.c	6.a
7.d	8.b	9.b	10.d	11.d	12.d
13.b	14.a	15.			

MOS Transistors as Switches

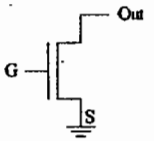


*n*MOS transistor:
Closed (conducting) when Gate = 1 (V_{DD})
Open (non-conducting) when Gate = 0 (ground, 0V)



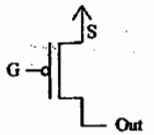
*p*MOS transistor:
Closed (conducting) when Gate = 0 (ground, 0V)
Open (non-conducting) when Gate = 1 (V_{DD})

For *n*MOS switch, source is typically tied to ground and is used to *pull-down* signals:



when Gate = 1, Out = 0, (0V)
when Gate = 0, Out = Z (high impedance)

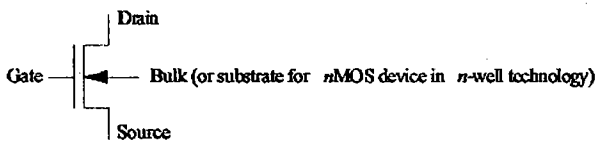
For *p*MOS switch, source is typically tied to V_{DD}, used to *pull* signals *up*:



when Gate = 0, Out = 1 (V_{DD})
when Gate = 1, Out = Z (high impedance)

Note: The MOS transistor is a symmetric device. This means that the drain and source terminals are interchangeable. For a conducting *n*MOS transistor, V_{DS} > 0V; for the *p*MOS transistor, V_{DS} < 0V (or V_{SD} > 0V).

Basic MOS Device Equations



The *n*MOS device is a *four* terminal device: Gate, Drain, Source, Bulk.

Bulk (substrate) terminal is normally ignored at schematic level, usually tied to ground for the *n*MOS case. In analog applications, however, the bulk terminal may not be ignored.

Gate controls channel formation for conduction between Drain and Source. Drain at higher potential than Source — Source usually tied to GND to act as pull-down (*n*MOS).

Three regions of operations — first-order (*ideal*) equations:

Cutoff region

$I_D = 0A$ $\qquad V_{GS} \le V_{Tn}$ (*n*MOS threshold voltage)

Linear region

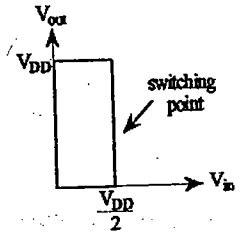
$$I_D = \beta\left[(V_{GS} - V_{Tn})V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad 0 < V_{DS} < V_{GS} - V_{Tn}$$

Note: I_D is linear with respect to $(V_{GS} - V_{Tn})$ only when $(V_{DS}^2/2)$ is small.

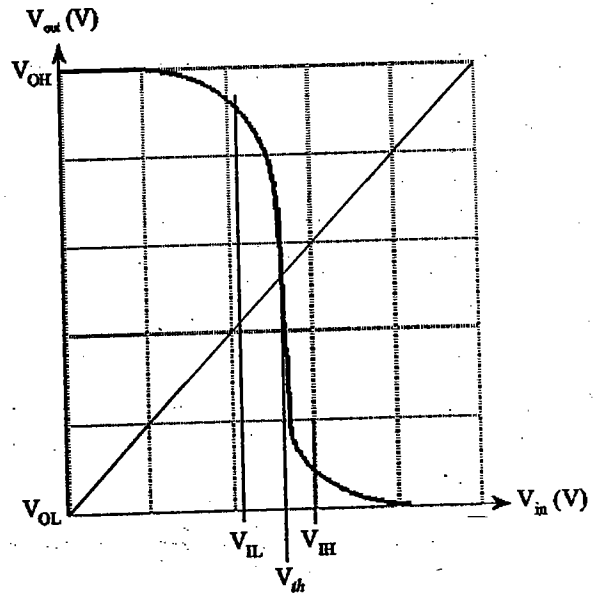
Saturation region

$$I_D = \frac{\beta}{2}(V_{GS} - V_{Tn})^2 \qquad 0 < V_{GS} - V_{Tn} < V_{DS}$$

Ideal Inverter

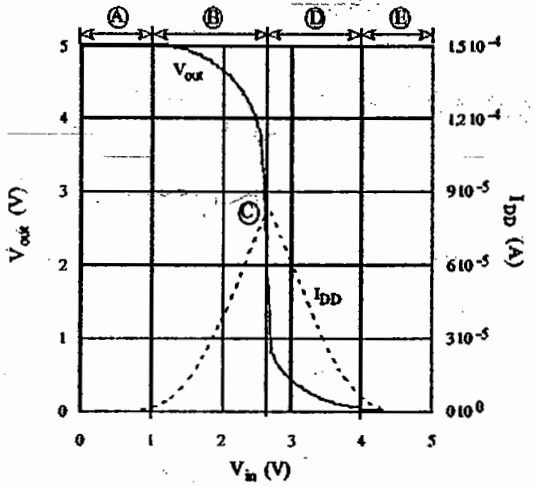


Actual Inverter Characteristics, some definitions



- V_{IL} represents the maximum logic 0 (LOW) input voltage that will guarantee a logic 1 (HIGH) at the output
- V_{IH} represents the minimum logic 1 (HIGH) input voltage that will guarantee a logic 0 (LOW) at the output

CMOS Inverter Regions of Operation



Region A:

$0 \le V_{in} < V_{Tn}$ $\Rightarrow$ *p*MOS nonsaturated (cutoff); *n*MOS cutoff

- *n*MOS is cutoff because $V_{in} < V_{Tn}$

Why is the *p*MOS device in the linear region?

Linear region $\equiv$ $V_{SDp} < V_{SGp} - |V_{Tp}|$

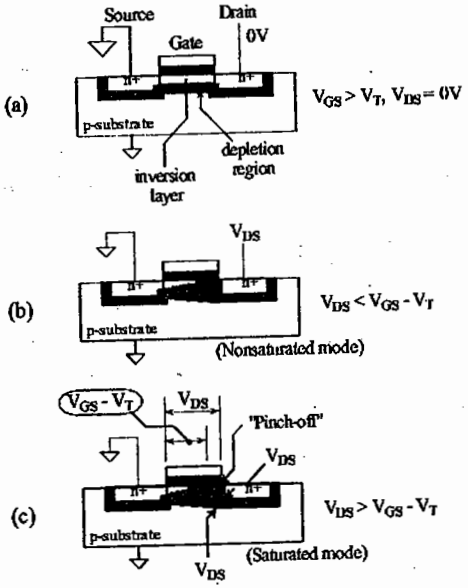
$(5 - 5)V < (5 - 0)V - |-0.7|V$

[for $V_{DD} = 5V$ and $V_{Tp} = -0.7V$]

$0V < 4.3V$

Note that the *p*MOS device can be in linear region even if $I_{Dp} \equiv 0A$!

MOSFET Structure versus Bias



Cross-section (a): potential in channel same everywhere because $V_{GS} = V_{GD}$, channel "depth" same everywhere since $V_{GS} > V_T$ and $V_{GD} > V_T$

Cross-section (b): Depth of channel varies somewhat linearly with V_{GS} *and* V_{DS}. As V_{DS} is increased, the drain-side of channel (just beneath the gate) becomes "pinched" because V_{GD} becomes less and less.

Cross-section (c): Here the current depends only on V_{GS} and not V_{DS} (if we neglect channel-length modulation) and the channel becomes completely pinched-off near the drain. With $V_{DS} > V_{GS} - V_T$ but $V_S = 0V$, then $V_D > V_G - V_T$ and hence, $V_T > V_{GD}$, i.e., $V_{gate\text{-}to\text{-}drain}$ is less than the threshold voltage.

How does conduction occur *after* "pinch-off"? Electrons enter channel from source, then are swept across depletion region near drain by the positive drain voltage with respect to source (V_{DS}).

MOSFET Threshold Voltage

$V_T = V_{T\text{-}MOS} + V_{FB}$ ($V_{T\text{-}MOS}$ is positive for *n*MOS, negative for *p*MOS)

$V_{T\text{-}MOS}$ — ideal threshold voltage for a MOS capacitor (the capacitor formed between the gate and substrate)

V_{FB} — Flatband voltage

$V_{T\text{-}MOS} = 2\phi_b + \frac{Q_b}{C_{ox}}$ (Note: "Q_b" sometimes referred to as "Q_{bo}")

$\phi_b = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$ ⇐ bulk Fermi potential

C_{ox} = oxide capacitance, inversely proportional to oxide thickness $\left(C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}\right)$

$Q_b = \sqrt{2\epsilon_{si} q N_A 2\phi_b}$ ⇐ bulk charge term (total charge stored in depletion layer), *p*-substrate in this case

Bulk potential — potential difference between Fermi level in intrinsic semiconductor and Fermi level in doped semiconductor

Fermi level is the average energy level in a material. For intrinsic materials, it is halfway between the valence band and conduction band.

p-type ⇒ Fermi level closer to valence band

n-type ⇒ Fermi level closer to conduction band

Other Constants (see text for values):

k = Boltzmann's constant (eV/K, J/K)

q = Electronic charge (coulombs)

T = temperature (°K)

N_A = carrier density in doped semiconductor

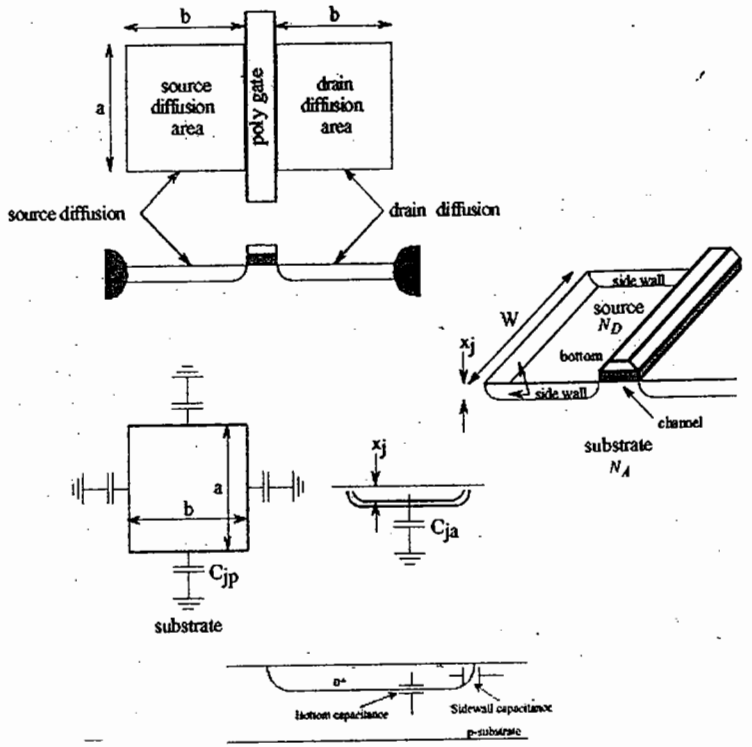
n_i = intrinsic carrier concentration in Silicon

ϵ_{si} = permittivity of Silicon = $\epsilon_r \cdot \epsilon_o$

ϵ_r = 11.7 (relative Silicon permittivity)

ϵ_o (permittivity of free space)

Source/Drain Capacitance



Two components:

C_{bottom} ⇒ diffusion area to substrate

$C_{sidewall}$ ⇒ diffusion depth × peripheral area

C_{ja} = junction capacitance per μm^2

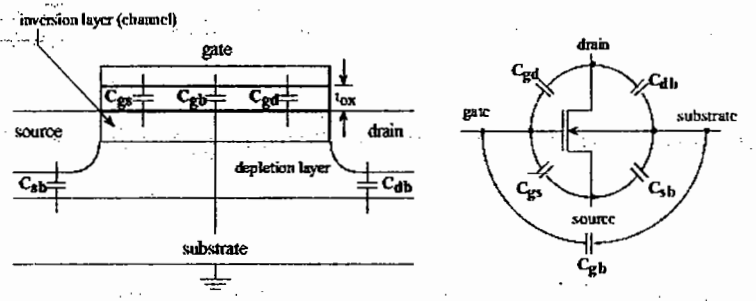
C_{jp} = periphery capacitance per μm

$C_{diff} = C_{bottom} + C_{sw}$

$= C_{ja} \times \text{area} + C_{jp} \times \text{perimeter}$

$= C_{ja} \times a \times b + C_{jp} \times (2a + 2b)$

MOS Device Capacitance Estimation



In cutoff region, gate-to-channel capacitance composed entirely of C_{gb} where

$$C_{gb} = C_{ox}WL_{eff}$$

$$C_{ox} = \frac{e_o e_{SiO_2}}{t_{ox}}$$

where ε_o is free space permittivity and e_{SiO_2} relative permittivity for SiO_2

When channel is formed, depletion layers blocks C_{gb}.

In linear region, C_{gb} blocked by formation of channel and gate-to-channel capacitance split evenly between C_{gs} and C_{gd} where

$$C_{gs} = C_{gd} = \frac{1}{2}C_{ox}WL_{eff}$$

In saturation, channel is pinched off at drain, so $C_{gd} \approx 0$, $C_{gs} \approx \frac{2}{3}C_{ox}WL_{eff}$

Average channel capacitances of MOSFETs for different operation regions:

Region of operation	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	~0	~0
Linear	~0	$(1/2)C_{ox}WL_{eff}$	$(1/2)C_{ox}WL_{eff}$
Saturation	~0	$(2/3)C_{ox}WL_{eff}$	~0

$$C_g = C_{gb} + C_{gs} + C_{gd}$$

Typical diffusion capacitance values for a 1 μm *n*-well process:

	n-device (or wire)	*p*-device (or wire)
C_{je}	3×10^{-4} pF/μm^2	5×10^{-4} pF/μm^2
C_{jp}	4×10^{-4} pF/μm	4×10^{-4} pF/μm

The source/drain areas from *p/n* junctions with substrate or well. The junction voltage will affect the capacitance, both C_{je} and C_{jp}

General expression:

$$C_j = \frac{C_{je}}{\left(1 - \frac{V_j}{V_b}\right)^m}$$

where

V_j = junction voltage, negative for reverse bias

C_{jo} = zero bias capacitance

V_b = built-in junction potential (≈0.6V)

m = grading coefficient (typical values between 0.3 and 0.5)

OBJECTIVE

01. In integrated circuits, the design of electronic circuits is based on the approach of use of
(a) maximum number of resistors in the circuits
(b) large sized capacitor
(c) minimum chip area irrespective of the type of components in the design
(d) use of only bipolar transistors

02. The basic function of buried n^+ layer in an n- p- n transistor fabricated in IC is to
(a) Reduce the magnitude of the base spreading resistance
(b) Reduce the collector series resistance
(c) Reduce the base width of the transistor
(d) Increase the gain of the transistor

03. The p-type substrate in a conventional p-n junction isolated integrated circuit should be connected to
(a) no where i.e. left floating
(b) a d.c. ground potential
(c) the most positive potential available in the circuit
(d) the most negative potential available in the circuit

04. For a MOS capacitor fabricated on a p-type semiconductor, strong inversion occurs when
(a) Surface potential is equal to fermi potential.
(b) Surface potential is negative fermi potential.
(c) Surface potential is positive and equal to twice the fermi potential
(d) Surface potential is negative and equal to fermi potential in magnitude.

05. Almost all resistors are made in a monolithic integrated circuit
(a) during the emitter diffusion
(b) while growing the epitaxial layer
(c) during the base diffusion
(d) during the collector diffusion

06. An I.C. operational amplifier has a typical open loop gain of 1200 and the common mode rejection of 55 dB. What is the common mode rejection of Ratio (CMRR)?
(a) 550 (b) 560 (c) 570 (d) 580

07. Match List-I (Isolation Technique in IC) with List-II (Related Characteristic) and select the correct answer using the code given below the lists:

List-I

A. Reverse bias p-n junction isolation
B. Resistive isolation using the bulk resistivity of the layer
C. Native oxide isolation
D. Oxide (other than native)

List-II

1. Requires large area of the water, thereby increasing the IC size
2. Best choice for silicon ICs with low parasitic capacitance
3. Suitable for ICs of III-V semiconductors
4. Introduces bias-dependent parasitic capacitance

Code :	A	B	C	D
(a)	4	1	2	3
(b)	2	3	4	1
(c)	4	3	2	1
(d)	2	1	4	3

KEYS:

01. c 02. b 03. d 04. d 05. a
06. b 07. a

PREVIOUS IES QUESTIONS:

01. In an integrated circuit, the SiO_2 layer provides
(a) electrical connection to external circuit
(b) physical strength
(c) isolation
(d) conducting path

02. In the fabrication of a buried layer n-p-n transistor, the processes involved are
1. diffusion
2. oxidation
3. epitaxy
4. lithography
The correct sequence in which these processes are to be carried out, is
(a) 2, 4, 3, 1 (b) 4, 2, 1, 3
(c) 2, 4, 1, 3 (d) 4, 2, 3, 1

03. In switching diode fabrication, dopant is introduced into silicon which introduces additional trap levels in the material thereby reducing the mean life time of carriers. This dopant is
(a) Aluminium (b) Platinum
(c) Gold (d) Copper

04. The scaling factor of a MOS device is α. Using constant voltage scaling model, the gate area of the device will be scaled as (a) $1/\alpha$ (b) $1/\alpha^2$
(c) $1/\alpha^3$ (d) $1/\alpha^4$

05. A CMOS amplifier when compared to an N-channel MOSFET, has the advantage of
(a) Higher cut-off frequency
(b) Higher voltage gain
(c) Higher current gain
(d) Lower current drain from the power supply, therby less dissipation.

06. In fabricating silicon BJT in ICs by the epitaxial process, the number of diffusions used is usually
(a) 2 (b) 3 (c) 4 (d) 6

07. In the fabrication of n-p-n transistor in an IC, the buried layer on the p-type substrate is
(a) p^+ - doped
(b) n^+ - doped
(c) Used to reduce the parasitic capacitance
(d) Located in the emitter region.

08. Which one of the following statements is correct?
In the context of IC fabrication, metallization means
(a) connecting metallic wires
(b) formation of interconnecting conduction pattern and bonding pads
(c) doping SiO_2 layer
(d) covering with a metallic cap

09. Which one of the following statements is correct?
For an MOS capacitor fabricated on a p- type semiconductor. strong inversion occurs when surface potential is
(a) equal to Fermi potential
(b) zero
(c) negative and equal to Fermi potential in magnitude
(d) positive and equal to Fermi potential in magnitude

10. Diffusion of impurities in a semiconductor is carried out in a furnace through which a steady stream of impurity atoms is passed during the entire diffusion process. What would be the type of profile of the impurity atom inside the semiconductor?
(a) Linear
(b) Gaussian
(c) Complementary error function
(d) Exponential

11. Match **List-I** (Isolation Technique in IC) with **List-II** (Related characteristic) and select the correct answer using the codes given below the lists:

List-I

A. Reverse bias p-n junction isolation
B. Resistive isolation using the bulk resistivity of the layer
C. Native oxide isolation
D. Oxide(other than native isolation)

List-II

1. Requires large area of the wafer, thereby increasing the IC size
2. Best choice for silicon ICs with low parasitic capacitance
3. Suitable for IC of III-V semiconductors
4. Introduces bias-dependent parasitic capacitance

Codes:

	A	B	C	D
(a)	4	1	2	3
(b)	2	3	4	1
(c)	4	3	2	1
(d)	2	1	4	3

12. Consider the following statements Related to a CMOS (Complementary metal oxide semiconductor) inverter:

1. It combines an n – channel and a p – channel MOS transistor
2. For binary 1 input, both transistors are OFF
3. For binary 0 input, both transistors are ON
4. Whatever is the state of input , one transistor is ON while the other is OFF.

Which of the statements given above are correct?

(a) 1, 2, 3 and 4
(b) 1 and 4
(c) 1, 2 and 3
(d) 3 and 4.

13. The basic function buried n^+ layer in an n – p – n transistor in IC is to

(a) Reduce the magnitude of the base spreading resistance
(b) Reduce the collector series resistance
(c) Reduce the base width of the transistor
(d) Increase the gain of the transistor

14. Which one of the statements concerning IC fabrication is not correct?

(a) A typical wafer of doped Si may be 400 μm thick, of diameter 5 – 15 cm. The purity of the wafer does not matter and can be even polycrystalline in nature.

(b) Resistors are obtained by utilizing the bulk resistivity of one of the regions; for example, the DS channel of MOSFET can serve as a resistor.

(c) Semiconductors lack magnetic properties, so they cannot exhibit inductance. However, the inductors can be realized by combination of active and passive components.

(d) in a reverse biased p –n junction, the positive and negative ions exist on opposite sides of the p – n junction; because of that p – n junction behaves like a parallel plate capacitor

15. **Assertion (A):** The resistors and capacitors fabricated using IC technology have poor tolerances with respect to their absolute values.

Reason (R): As all the components of the IC are fabricated simultaneously, their ratio of tolerances is very low.

(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

16. Which of the following capacitors are made use of widely for a capacitance application in monolithic ICs.

1. MOS capacitor
2. Collector Substrate capacitor
3. Collector – Base capacitor
4. Base – Emitter capacitor

Select the correct answer using the code given below.

(a) 1 and 2 only (b) 2 and 3 only
(c) 3 and 4 only (d) 1 and 4 only

17. why is silicon dioxide(SiO_2) layer used in ICs?

(a) To protect the surface of the chip from external contaminants and to allow for selective formation of the n and p regions by diffusion
(b) Because it facilitates the penetration of the desired impurity by diffusion
(c) To control the concentration of the diffused impurities
(d) Because of its high heat conduction

18. Why is the term 'plainer technology' for fabrication of devices in ICs used?

(a) The variety of manufacturing processes by which devices are fabricated, takes place through a single plane
(b) The aluminum contacts to the collector, base and emitter regions of the transistors in the ICs are laid in the same plane
(c) The collector, base and emitter regions of the transistors in ICs are laid in the same plane
(d) The device looks like a thin plane wafer

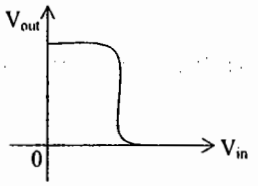
KEY:

1.c	2.d	3.c	4.b	5.d	6.b
7.b	8.b	9.d	10.c	11.a	12.b
13.d	14.a	15.a	16.a	17.a	18.a

PREVIOUS GATE QUESTIONS:

KEY:
1.c 2.a 3.b

1. Given figure is the voltage transfer characteristic of **GATE - 2004**



(a) an NMOS inverter with enhancement mode transistor as load
(b) an NMOS inverter with depletion mode transistor as load.
(c) a CMOS inverter
(d) a BJT inverter

2. Which of the following is true?
(a) A silicon wafer heavily doped with boron is a p^+ substrate.
(b) A silicon wafer lightly doped with boron is a p^+ substrate.
(c) A silicon wafer heavily doped with arsenic is a p^+ substrate.
(d) A silicon wafer lightly doped with arsenic is a p^+ substrate.

3. If P is passivation, Q is n-well implant, R is metallization and S is source/drain diffusion, then the order in which they are carried out in a standard n-well CMOS fabrication process, is
GATE – 2003
(a) P – Q – R – S (b) Q – S – R – P
(c) R – P – S – Q (d) S – R – Q – p

CHAPTER – 5 BASICS OF OPTO ELECTRONICS

FUNDAMENTALS OF LIGHT

According to the Quantum Theory, light consists of discrete packets of energy called photons. The energy contained in a photon depends on the frequency of the light and is given by the relation **E=hf** where **h** is Plank's constant (6.625×10^{-34} Joule-second). In this equation, energy **E** is in Joules and frequency **f** is in hertz (Hz).

As seen, photon energy is directly proportional to frequency: higher the frequency, greater the energy. Now, velocity of light is given by **c=fλ** where **c** is the velocity of the light (3×10^8 m/s) and **λ** is the wavelength of light in meters. The wavelength of light determines its colour in the visible range and whether it is ultraviolet or infrared outside the visible range.

Now, $E = hf = hc/\lambda$ or $\lambda = hc/E$ meters
$\therefore \quad \lambda = 6.625 \times 10^{-34} \times 3 \times 10^8/E = 19.875 \times 10^{-26}/E$ --E in joules
If E is in electron-volt (eV), then since $1\ eV = 1.6 \times 10^{-19}$/E
$\therefore \quad \lambda = 19.875 \times 10^{-26}/E \times 1.6 \times 10^{-19} = 12.42 \times 10^{-7}/E$ meter --E in eV
or $\lambda = 1.242\ \mu m$

In a forward-biased p-n junction, electrons and holes both cross the junction. In the process, some electrons and holes recombine with the result that electrons lose energy. The amount of energy lost is equal to the difference in energy between the conduction and valence bands, this being known as the semiconductor energy band gap E_g. The value of E_g for silicon is 1.1eV, for GaAs is 1.43 eV and for INAs is 0.36 eV.
For example, the wavelength of light emitted by silicon p-n junction is

$$\lambda = 1.242/E_g = 1.242/1.1 = 1.13\ \mu m.$$

PHOTODIODES

Photodiode is a special type of photo-detector. The general principle of all semiconductor-based photo detectors is the electron-excitation from the valence band to the conduction band by photons.
Suppose an optical photon of frequency ν is incident on a semiconductor, such that its energy is greater than the band gap of the semiconductor (i.e., $h\nu > E_g$).

This photon will excite an electron from the valence band to the conduction band leaving a vacancy or hole in the valence band. Thus, an electron-hole pair is generated. These are additional charge carriers termed as photo generated charge carriers which obviously increase the conductivity of the semiconductor.

Larger the number of incident photons (incident intensity of light), larger would be the change in the conductivity of the semiconductor, one can measure the intensity of the optical signal. Such photo detectors are known as photoconductive cells. However, more commonly used photo detecting devices are "photodiodes".

You already know that at the p-n junction there exists a junction field which, at equilibrium, does not permit the flow of charge carriers across the junction. The current can only flow with applied bias.

The diodes are generally reverse biased when used as photodiode. Suppose such a p-n diode is illuminated with light photons having energy $h\nu > E_g$. The electron and hole pairs

generated in the depletion layer (or near the junction) will be separated by the junction field and made to flow across the junction.

A measurement of the change in the reverse saturation current on illumination can give the values of the light intensity.

The dark current refers to the current that flows when no light is incident. By changing the illumination level, reverse current can be changed. In this way, reverse resistance of the diode can be changed by a factor of nearly 20.

A photodiode can turn its current ON and OFF in nanoseconds. Hence, it is one of the faster photo detectors. It is used where it is required to switch light ON and OFF at a maximum rate.

APPLICATIONS:

1. Detection, both visible and invisible;
2. Demodulation;
3. Switching;
4. Logic circuit that require stability and high speed;
5. Character recognition;
6. Optical communication equipment;
7. Encoders etc.

PIN Photo detector:

When a light intensity of wavelength λ is incident on the photo diode ,if energy $E_\lambda > E_G$ of PIN Diode then a output current 'I_p'in response to the incident light is produced.

Quantum efficiency of PIN diode is given by $\eta = \dfrac{\text{No of electron hole pairs generated}}{\text{No of photons incidented}}$

$$\eta = \frac{(I_p / q)}{(P_0 / hf)}$$

Responsivity $R = I_p / P_0 = (\eta q) / (hf)$ A / watt

Maximum wavelength $\lambda_{max}(\mu m) = \dfrac{1.24}{E_g(ev)}$ $\lambda_{max}(A^0) = \dfrac{12400}{E_g(ev)}$

f = frequency of incident photon
P_0 = incident optical power
I_p = Photocurrent generated in PIN diode
Disadvantage of photo diode is low output current.

Avalanche Photo Diode:

Avalanche photo diode is also a photo detector. A photo diode will produce less amount of current, which is not sufficient to drive some circuits. An Avalanche photodiode gives more output current when compared to a photo diode. The output current in an Avalanche photo diode is equal to M times the output current of a photo diode that is produced due to "impact ionization".

LIGHT EMITTING DIODE (LED)

These are forward-biased p-n junctions which emit spontaneous radiation. You know that radiation is emitted whenever an exited electron falls from higher excited energy state to a lower energy state.

You know that there are two distinct energy bands in a semiconductor, the conduction (higher energy) and the valence (lower energy) bands. There may also be energy bands due to donor impurities (E_D) near the conduction band or acceptor impurities (E_A) near the valence band. When electron falls from the higher to lower energy level containing holes, the energy in the form of light radiation is released. Generally, radiations transitions occur (sometimes non-radiative transition may also occur).

The energy of radiation emitted by LED is equal to or less than the band gap of the semiconductor used.

The semiconductor used in LED is chosen according to the required wavelength of emitted radiation. Visible LED's are available for red, green and orange. The visible wavelength is from 0.45 μm to 0.7 μm (Energy 2.8 eV to 1.8 eV). Therefore, the least band gap of the semiconductor for use in the visible region is 1.8 eV. Phosphorous doped (GaAs P) and GaP are the preferred materials. Obviously, Si ($E_g \sim 1.1$eV) or Ge($E_g \sim 0.7$eV) are not suitable, since E_g is less than the minimum required E_g of ~ 1.8eV.

GaAs (with $E_g \sim 1.5$ eV) alone or in conjunction with aluminum doped GaAs (AlGaAs) are commonly used for infrared LED's.

The color of the emitted light depends on the type of material used is given below:

1. GaAS – infrared radiation (invisible)
2. GaP – red or green light.
3. GaAsP – red or yellow(amber) light.

LEDs emit no light when reverse-biased. In fact, operating LEDs in reverse direction will quickly destroy them.

A metal (gold) film is applied to the bottom of the substrate for reflecting as much light as possible to the surface of the device and also to provide cathode connection. LEDs are always encased in order to protect their delicate wires.

Applications:

To choose emitting diodes for a particular application, one or more of the following points have to be considered: wavelength of light emitted, input power required, output power, efficiency, turn-on and turn-off time, mounting arrangement, light intensity and brightness etc.

Since LEDs operate a voltage levels from 1.5 V to 3.3 V, they are highly compatible with solid-state circuitry.

Their uses include the following:

1. LEDs are used in burglar-alarm systems
2. for solid-state video displays which are rapidly replacing cathode-ray tubes(CRT);
3. In image sensing circuits used for 'picturephone';

4. in the field of optical communication where high-radiance GaAs diodes are matched into the silica-fiber optical cable;
5. in arrays of different types for displaying alphanumeric (Letters and numbers) or supplying input power to lasers or for entering information into optical computer memories;
6. for numeric display in hand-held or pocket calculators.

LASER DIODE

The word LASER is an acronym and stands for light amplification by stimulated emission and radiation, which sums up the operation of an important optical and electronic device. The laser is a source of highly directional, monochromatic, and coherent light.

It is an interesting variant of LED in which its special construction helps to produce stimulated radiation as in laser. In conventional solid state or gas laser, discrete atomic energy levels are involved while in semiconductor lasers, the transitions are associated with the energy bands of the semiconductor.

The primary requirement is the population inversion, i.e., the higher energy level is more populated than the lower energy level. The situation for the forward biased p-n junction of LED is similar. Due to the dc bias, the electrons go to the higher energy level (i.e., conduction band).

When a photon of energy $h\nu = E_g$ impinges the device, while it is still in the excited state due to the applied bias, the system is immediately stimulated to make its transition to the valence band and gives an additional photon of energy $h\nu$ which is in phase with the incident photon.

When a forward bias is applied, a current flows. Initially at low current, there is "spontaneous emission" (as in LED) in all the directions. Further, as the bias is increased, a threshold current is reached at which the "stimulated emission" occurs. Diode lasers are low power lasers used as optical light source in optical communication.

Unique Characteristics of Laser Light:

The beam of laser light produced by the diode has the following unique characteristics:

1. it is coherent i.e. there is no path difference between the waves comprising the beam.
2. it is monochromatic i.e. it consists of one wavelength and hence one color only;
3. it is collimated i.e. emitted light waves travel parallel to each other.

Laser diodes have a threshold level of current above which the laser action occurs but below which the laser diode behaves like a LED emitting coherent light. Incidentally, a filter or lens is necessary to view the laser beam.

OBJECTIVE - 1

01. When a p-n junction is formed, diffusion current causes
a) mixing of current carriers
b) forward bias
c) reverse bias
d) barrier potential

02. The leakage current of a p-n diode is caused by
a) heat energy b) chemical energy
c) barrier potential d) majority carriers

03. Electronic components which are made of a semiconductor material are often called ..... devices
a) solid -- state b) silicon
c) germanium d) intrinsic

04. The area within a semiconductor diode where no mobile current carriers exist when it is formed is called ... region.
a) depletion b) saturation
c) potential barrier d) space charge

05. The depletion region of a semiconductor diode is due to
a) reverse biasing
b) forward biasing
c) crystal doping
d) migration of mobile charge carriers

06. The width of depletion layer of a p-n Junction
a) decreases with light doping
b) increases with heavy doping
c) is independent of applied voltage
d) is increased under reverse bias

07. LEDs are commonly fabricated from gallium compounds like gallium arsenide and gallium phosphide because they
a) are cheap
b) are easily available
c) emit more heat
d) emit more light

08. A LED is basically a ..... p-n junction
a) forward biased
b) reverse biased
c) lightly doped
d) heavily doped

09. As compared to a LED display, the distinct advantage of an LCD display is that it requires
a) no illumination
b) extremely low power
c) no forward bias
d) a solid crystal

10. Before illuminating a p-n junction photodiode, it has to be
a) reverse biased
b) forward biased
c) switched ON
d) switched OFF

11. A phototransistor excels a photodiode in the matter of
a) faster switching
b) greater sensitivity
c) higher current capacity
d) both (a) and (b)
e) both (b) and (c)

12. The unique characteristics of LASER light are that it is
a) coherent
b) monochromatic
c) collimated
d) all of the above

13. Silicon is preferred for manufacturing Zener diodes because it
a) is relatively cheap
b) needs lower doping level
c) has higher temperature and current capacity
d) has lower break -- down voltage

14. A PIN diode is frequently used as a
a) peak clipper
b) voltage regulator
c) harmonic generator
d) switching diode for frequencies upto GHz range

15. A diode that has no depletion layers and operates with hot carriers is called ..... Diode
a) Schottky b) Gunn
c) step recovery d) PIN

16. The junction capacitance of a p-n junction depends on
a) Doping concentration only
b) Applied voltage only
c) Both doping concentration and applied voltage
d) Barrier potential only

17. When a junction diode is used in switching applications, the forward recovery time is:
a) Of the order of the reverse recovery time
b) Negligible in comparison to reverse recovery time
c) Greater than the reverse recovery time
d) Equal to the mean carrier life time τ for the excess minority carriers

18. In a degenerate semiconductor, the majority carriers are controlled by
a) Fermi – dirac statistics
b) Maxwell – Boltzmann statistics
c) Bose – Einstein (B – E) statistics
d) Pauli's exclusion principle

19. In a forward biased photo diode, an increase in incident light intensity causes the diode current to
a) Increases
b) Remains constant
c) Decreases
d) Remaining constant, the voltage drop across the diode increases

20. For a junction diode, which one of the following statement is false
a) the depletion capacitance increases with increase in the reverse bias
b) the depletion capacitance decreases with increase in the reverse bias
c) the diffusion capacitance increases with increase in the forward bias
d) the diffusion capacitance is much higher than the depletion capacitance when it is forward biased.

21. In an unbiased p-n junction, the junction current at equilibrium is
a) due to diffusion of minority carriers only
b) due to diffusion of majority carriers only
c) zero, because equal but opposite carriers are crossing the junction
d) zero, because no charges are crossing the junction

22. Semiconductor diode time constant is equal to
a) the value of majority carrier life time
b) the life time of minority carrier
c) the diffusion capacitance time constant
d) zero

23. The reverse current of a silicon diode is
a) Highly bias voltage sensitive
b) Highly temperature sensitive
c) Both bias voltage and temperature sensitive
d) Independent of bias voltage and temperature

24. A combination of two diodes connected in parallel when compared to a single diode can withstand
a) Twice the value of peak inverse voltage
b) Twice the value of maximum forward current
c) A larger leakage current
d) Twice the value of cut-in voltage

25. When a p-type semi conductor material is bonded to an n-type semi conductor material and terminals are added, the resulting structure does not have the property that
a) Ideally, the forward bias resistance is zero
b) As temperature is increased above room temperature, the material resistance decreases because the doping material charges are " freed "
c) Both holes and electrons contribute to the current flow
d) The resistance increases with increasing doping

26. Depletion capacitance in a diode depends on
1 Applied junction voltage
2. Junction built-in potential
3 Current through junction
4. Doping profile across the junction
Select the correct answer using codes given below:
a) 1 and 2 b) 1 and 3
c) 1,2 and 4 d) 2,3 and 4

27. The diffusion capacitance of a p-n junction diode
a) Increases exponentially with forward bias voltage
b) Decreases exponentially with forward bias voltage
c) Decreases linearly with forward bias voltage
d) Increases linearly with forward bias voltage

28. A zener diode works on the principle of
a) tunneling of charge carriers across the junction
b) thermionic emission
c) diffusion of charge carriers across the junction
d) hopping of charge carriers across the junction

29. The sensitivity of a photo diode depends upon
a) light intensity and depletion region width
b) depletion region width and excess carrier life time
c) excess carrier life time and forward bias current
d) forward bias current and light intensity

30. Avalanche photo diodes are preferred over PIN diodes in optical communication systems because of
a) speed of operation
b) higher sensitivity
c) larger bandwidth
d) larger power handling capacity

ANSWERS

(1)d (2)a (3)a (4)a (5)d (6) d (7) d (8) a (9) b (10)a (11) c (12)d 13)c (14) d (15)b (16)c (17)b (18)a (19)d (20)a (21) c (22) b (23) b (24) c (25) d (26) c (27) (28) c (29) a (30) d

OBJECTIVE - 2

01. A hetero – structure laser is better than a diode laser (injection laser) because of
(a) Low cost
(b) Long wavelength emission
(c) Low threshold current
(d) Non-linear operation

02. Given that the band gap of cadmium sulphide is 2 5 eV, the maximum photon wavelength for electron hole pair generation will be
(a) 5400μ *m* (b) 540μ *m*
(c) 5400A^0 (d) 540A^0

03. Avalanche photodiodes are preferred over PIN diodes in optical communication system because of
(a) Speed of operation
(b) higher sensitivity
(c) larger bandwidth
(d) larger powe handling capacity

04.. In forward biased photo diode with increase in incident light intensity, the diode current
(a) increase
(b) remain constant
(c) decrease
(d) remaining constant, the voltage drop across the diode increases

05. Photons of energy 1.53X10^{-19} Joules are incident on a photodiode which has a responsivity of 0.65 A/W. If the optical power level is 10μW, what is the photo current generated?
(a) 64μA (b) 1.5μA
(c) 2.1μA (d) 6.5 μA

KEYS :

01. c	02. c	03. d
04. a	05. d	

PREVIOUS IES QUESTIONS:

01. Almost all resistors are made in a monolithic integrated circuit.
(a) during the emitter diffusion.
(b) while growing the epitaxial layer
(c) during the base diffusion
(d) during the collector diffusion.

02. Consider the following statements:
Impurity diffusion is need in semiconductor to control the conductivity. The nature of the impurity profile should be such that the
1. impurity concentration decreases with diffusion depth.
2. profile results in an internal electric field.
1. impurity concentration is homogeneous with no internal electric field.
Which of these statements are correct?
(a) 1, 2 and 3 (b) 1 and 3
(c) 2 and 3 (d) 1 and 2

03. Which one of the following statements is correct in respect of the use of Direct Gap (DG) and Indirect Gap (IG) semiconductors in fabrication of Light Emitting diode?
(a) Both DG and IG semiconductors are suitable
(b) Only DG semiconductor is suitable
(c) DG semiconductor is suitable and some IG materials having proper dopants are also used
(d) only IG semiconductors are suitable

04. Consider the following statements in relation to a semiconductor laser diode:
1. The material should be a direct gap semiconductor
2. Some form of wavelength selective structure or resonator must be present.
3. Light output increases linearly with bias current.
4. Light output increase significantly when bias current exceeds a threshold value
Which of the statements given above are correct?
a) 1,2 and 4 b) 1 and 3
c) 2 and 4 d) 2 and 3

05. Photons of energy 1.53 × 10^{-19} Joule are incident on a photodiode which has a responsivity of 0.65 A/W. If the optical power level is 10 μW, what is the photocurrent generated?
(a) 64 μA (b) 1.5 μA
(c) 2.1 μA (d) 6.5μA

06. Consider the following statements used in respect of the phenomenon – Population Inversion:
1. It means population in a higher state is higher than that in a lower state
2. It is observed under thermal equilibrium
3. It increases the rate of spontaneous emission
4. It increases the rate of stimulated emission
Which of the statements given above are correct?
(a) 1, 2 , 3 and 4 (b) Only 2 and 3
(c) Only 1 and 3 (d) Only 1 and 4

KEY:

1.c	2.d	3.b	4.a
5.d	6.d		

PREVIOUS GATE QUESTIONS:

1. Match items in Group 1 with items in Group 2, most suitably.

Group 1
P. LED
Q. Avalanche Photodiode
R. Tunnel diode
S. LASER

Group 2
1. Heavy doping
2. Coherent radiation
3. Spontaneous emission
4. Current gain

GATE – 2003
(a) P – 1; Q – 2; R – 4; S – 3
(b) P – 2; Q – 3; R – 1; S – 4
(c) P – 3; Q – 4; R – 1; S – 2
(d) P – 2; Q – 1; R – 4; S – 3

2. A particular green LED emits light of wavelength 5490 A. The energy handgap of the semiconductor material used there is (Planck's constant = 6.626 x 10^{-34} J–s)

GATE - 2003
(a) 2.26 eV (b) 1.98 eV
(c) 1.17 eV (d) 0.74 eV

3. The longest wavelength that can be absorbed by silicon, which has the bandgap of 1.12 eV, is 1.1 μm. If the longest wavelength that can be absorbed by another material is 0.87 μm, then the bandgap of this material is **GATE – 2004**
(a) 1.416 eV (b) 0.886 eV
(c) 0.854 eV (d) 0.706 eV

4. Find the correct match between Group 1 and Group 2 **GATE – 2006**

Group 1
E. Varactor diode
F. PIN diode
G. Zener diode
H. Schottky diode

Group 2
1. Voltage reference
2. High-frequency switch
3. Tuned circuits
4. Current controlled attenuator

(a) E-4, F-2, G-1, H-3
(b) E-2, F-4, G-1, H-3
(c) E-3, F-4, G-1, H-2
(d) E-1, F-3, G-2, H-4

5. Group I lists four types of p-n junction diodes. Match each device in Group I with one of the options in Group II to indicate the bias condition of that device in its normal mode of operation.

GATE - 2007

Group I
P. Zener Diode
Q. Solar cell
R. LASER diode
S. Avalanche Photodiode

Group II
1. Forward bias
2. Reverse bias

(a) P-1, Q-2, R-1, S-2
(b) P-2, Q-1, R-1, S-2
(c) P-2, Q-2, R-2, S-1
(d) P-2, Q-1, R-2, S-2

6. Group I lists four different semiconductor devices. Match each device in Group I with its characteristic property in Group II.

GATE - 2007

Group - I
P. BJT
Q. MOS capacitor
R. LASER diode
S. JFET

Group – II
1. Population inversion
2. Pinch-off voltage
3. early effect
4. Flat-band voltage

(a) P-3, Q-1, R-4, S-2
(b) P-1, Q-4 R-3, S-2
(c) P-3, Q-4, R-1, S-2
(d) P-3, Q-2, R-1, S-4

Key
1.c 2.a 3.a 4.c
5.b 6.c

SELF ASSESMENT QUESTIONS

TOPIC 1: SEMI CONDUCTORS

1. N – type silicon is obtained by doping silicon with
(A) germanium (B) aluminum (C) boron (D) phosphorous

2. The intrinsic carrier concentration of silicon sample at 300°K is 1.5×10^{16} /m^3. If after doping the number of majority carriers is 5×10^{20}/m^3, the minority carrier density is
(A) 4.5×10^{11}/m^3 (B) 3.33×10^{4}/m^3 (C) 5×10^{20}/m^3 (D) 3×10^{-5}/m^3

3. The band gap of silicon at 300°K is
(A) 1.36 ev (B) 1.10 ev (C) 0.80 ev (D) 0.67 ev

4. An n – type silicon bar has L = 0.1cm, A = 100μm^2, $N_D = 5 \times 10^{20}$ m^{-3}, $\mu_n = 0.13$ m^2/v sec, T = 300°K. Find R.
(A) $10^6\ \Omega$ (B) $10^4\ \Omega$ (C) $10^{-1}\ \Omega$ (D) $10^{-4}\ \Omega$

5. The Resistivity of a uniformly doped n – type silicon sample is 0.5 Ω cm. Given $\mu_n = 1250$ cm^2/v sec, $q = 1.6 \times 10^{-19}$C. Find donor impurity concentration in the sample
(A) 2×10^{16} / cm^3 (B) 1×10^{16} / cm^3 (C) 2.5×10^{15} / cm^3 (D) 5×10^{15} / cm^3

6. The concentration of minority carriers in an extrinsic semiconductor under equilibrium is
(a) directly proportional to the doping concentration
(b) inversely proportional to the doping concentration
(c) directly proportional to the intrinsic concentration
(d) inversely proportional to the intrinsic concentration

7. A heavily doped n-type semiconductor has the following data :

Hole-electron mobility ratio : 0.4
Doping concentration : 4.2×10^8 atoms/m^3
Intrinsic concentration : 1.5×10^4 atoms/m^3

The ratio of conductance of the n-type semiconductor to that of the intrinsic semiconductor of same material and at the same temperature is given by
(a) 0.00005 (b) 2,000 (c) 10,000 (d) 20,000

8. The conductivity of a semi conductor crystal due to any current carrier is NOT proportional to
(A) mobility of the carrier (B) effective densities of states
(C) electronic charge (D) surface states in semiconductor

9. A silicon sample A is doped with 10^{18} atoms/cm^3 of Boron. Another sample B of identical dimensions is doped with 10^{18} atoms/cm^3 of phosphorous. The ratio of electron to hole mobility is 3. the ratio of conductivity of sample A to B is
(A) 3 (B) 1/3 (C) 2/3 (D) 3/2

10. For a n – type semiconductors with $n = N_D$ and $p = n_i^2/N_D$. The hole concentration will fall below the intrinsic value because some of the holes
(A) drop back to acceptor impurity states (B) drop to donor impurity states
(C) virtually leave the crystal (D) recombine with electrons

11. Match List I with List II and select the correct answer using the codes given below the lists.

List I	List II
W. Drift current	1. Law of conservation of charge
X. Einstein's equation	2. Electric field
Y. Diffusion current	3. thermal voltage
Z. Continuity equation	4. Concentration gradient

(A) W X Y Z (B) W X Y Z (C) W X Y Z (D) W X Y Z
2 1 4 3 4 3 2 1 4 1 2 3 2 3 4 1

12. If an electric field is applied to an n – type semi conductor bar. The net current is
1. Due to both electrons & holes with electrons as majority carriers
2. The sum of electron & hole currents
3. The difference between electron and hole current
Which of the above statements (s) is true
(A) 1 alone (B) 1 & 2 (C) 2 alone (D) 3 alone

13. Drift current in a semi conductor is proportional to
(A) concentration gradient of charge carriers (B) concentration of charge carriers
(C) Inverse of cross sectional area of specimen (D) none

14. Which one of the following pairs of semi conductors and current carriers is correctly matched
(A) Intrinsic → Number of electrons = number of holes
(B) p – type → number of electrons > number of holes
(C) n – type → Number of electrons < number of holes
(D) metal → holes >> electrons

15. Match List I (crystal type) with List II(name of solid(D) and select the correct answer using the codes given below the lists.

List – I	List – II
W. Ionic	1. solid organ
X. Covalent	2. Copper
Y. Metallic	3. Silicon
Z. Vander wall's	4. Sodium chloride(Nacl)

(A) W–3, X– 4, Y–2, Z–1 (B) W–4, X–3, Y–I, Z–2
(C) W–3, X– 4, Y–1, Z–2 (D) W–4, X–3, Y–2, Z–1

16. The carrier mobility in a semi conductor is 0.4 m^2/v – sec. Its diffusion constant at 300°K will be (in m^2/sec)
(A) 0.43 (B) 0.16 (C) 0.04 (D) 0.01

17. At very high temperatures, extrinsic semi conductors become intrinsic because
(A) of drive in diffusion of dopants & carriers
(B) band to band transition dominates impurity ionization
(C) Impurity ionization dominates band to band transition
(D) band to band transition is balanced by impurity ionization

18. Which of the following elements acts as donor impurities
1. Gold 2. Phosphorous 3. Boron 4. Antimony 5. Arsenic 6. Indium
(A) 1, 2 & 3 (B) 1, 2, 4 & 6 (C) 3,4, 5 & 6 (D) 2,4, & 5

19. Measurement of hall coefficient in a semiconductor provides information on
(A) sign and mass of charge carriers (B) sign of charge carriers alone
(C) mass and concentration of charge carriers (D) sign and concentration of charge carriers

20. The hall constant in a p type – si bar is given by 5×10^3 cm^3/ coulomb. The hole concentration in bar is
(A) 1×10^{15} cm^{-3} (B) 1.25×10^{15} cm^{-3} (C) $1.5 \times 10^{15} cm^{-3}$ (D) 1.6×10^{15} cm^{-3}

21. Consider a semi conductor bar having square cross – section. Assume that the holes drift in the +ve x - direction and a magnetic field is applied perpendicular to the direction in which holes drift. The sample will show
(A) A –ve resistance in +ve y – direction (B) A +ve voltage in +ve y – direction
(C) A –ve voltage in +ve y – direction (D) A magnetic field in +ve y – direction

22. Electron mobility & life – time in a semiconductor at room temperature are respectively 0.36 m^2 / v-sec & 340 μs. The diffusion length is
(A) 3.13 mm (B) 1.77 mm (C) 3.55 mm (D) 3.13 mm

23. The electron and hole concentrations in an intrinsic semiconductor are n_i per cm^3 at 300k. Now, if acceptor impurities are introduced with a concentration of N_A per cm^3 (where $N_A >> n_i$), the electron concentration per cm^3 at 300k will be
(A) n_i (B) $n_i + N_A$ (C) $N_A - n_i$ (D) n_i^2 / N_A

24. Consider the following statements related to a semiconductor
1. Acceptor level lies close to valence bond
2. Donor level lies close to valence bond
3. n – type semi conductor behaves as a conductor at 0°K
4. p – type semi conductor behaves as an insulator at 0°K
(A) 2 & 3 are correct (B) 1 & 3 are correct (C) 1 & 4 are correct (D) 3 & 4 are correct

25. Silicon is doped with boron to a concentration of 4×10^{17} Atoms/cm^3. Assume intrinsic concentration of silicon as 1.5×10^{10} cm^{-3}. Compared to undoped silicon, the fermi level of doped silicon
(A) goes down by 0.13 ev (B) goes down by 0.427 ev
(C) goes up by 0.13 ev (D) goes up by 0.427 ev

Codes to be used for the following questions
a) Both A & R are true and R is correct explanation of A
b) Both A & R are true but R is not a correct explanation of A
c) A is true but R is false (D) A is false but R is true

26. **Assertion (A)** : Net charge with in a conductor is always zero
Reason (R) : The conductor has a very large number of free electrons

27. **Assertion (A)** : In hall effect, the open – circuit transverse voltage developed has opposite signs for n – type & p – type semiconductors.
Reason (R) : The magnetic field pushes both holes & electrons in the same direction.

28. **Assertion (A)** : At room temperature Fermi level in p – type semiconductor lies nearer the valence band, whereas in n – type semiconductor lies nearer the conduction-band.
Reason (R): At room temperature the p – type semiconductor is rich in holes whereas n – type is rich in electrons

Key:

1. d	2. a	3. b	4. c	5. b	6. b	7. d	8. d	9. b	10. d	11. d	12. b	13. b
14. a	15. d	16. d	17. b	18. d	19. d	20. b	21. b	22. b	23. d	24. c	25. b	26. b
27. c	28. a											

TOPIC 2: DIODES

1. At 300°K, for a diode current of 1mA, a certain germanium diode requires a forward bias of 0.1435V, whereas a certain silicon diode requires a forward bias of 0.718V. under the conditions stated above the closest approximation of the ratio of reverse saturation current in Ge diode to that in silicon diode is
(A) 1 (B) 5 (C) 4×10^3 (D) 8×10^3

2. In an abrupt PN junction the doping concentrations on the p – side and n – side are $N_A = 9 \times 10^{16}/m^3$, $N_D = 1 \times 10^{16}/cm^3$ respectively. The PN junction is reverse biased and total depletion width is 3μm. The depletion width on p side is
(A) 2.7 μm (B) 0.3 μm (C) 2.25 μm (D) 0.75 μm

3. Consider an abrupt p – n junction. Let V_{bi} be the built in potential of this junction and V_R be the applied reverse bias. If the junction capacitance (C_j) is 1pF for $V_{bi} + V_R = 1$v, then for $V_{bi} + V_r = 4$ v C_j will be
(A) 4 pF (B) 2 pF (C) 0.25 pF (D) 0.5 pF

4. The change is barrier potential of a si p – n junction diode with temperature is
(A) 0.0025 V/°C (B) 0.250 V/°C (C) 0.030 V/°C (D) 0.014 V/°C

5. A Si diode is carrying a constant current of 1mA. When the temperature of the diode is 20°C, V_D is found to be 700mV. If the temperature rises to 40°C V_D becomes approximately equal to
(A) 740 mV (B) 660 mV (C) 680 mV (D) 700 mV

6. The current I in a forward biased P^+N junction. Shown in figure-A is entirely due to diffusion of holes from x=0 to x=L. The injected hole concentration distribution in n-region is linear as shown in figure-B with $p(0) = 10^{12} cm^{-3}$ & $L = 10^{-3}$ cm. The current density in the diode assuming that the difussion coefficient of holes is $12 cm^2$/sec will be

Figure A

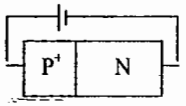
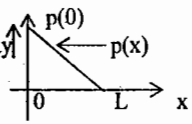


Figure B hole density



(A) 1.92 mA/cm^2 (B) 2.19 mA/cm^2 (C) 19.2 mA/cm^2 (D) 1.29 mA/cm^2

7. In the above problem velocity of holes in n-region at x = 0 will be
(A) 1200 cm/sec (B) 12×10^3 cm/sec (C) 12 cm/sec (D) 21 cm/sec

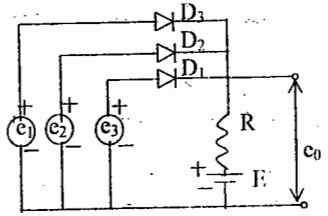
8. An one-sided abrupt junction has 10^{21} per m^3 of dopants on the lightly doped side. Builtin potential is 0.2V at zero bias. Depletion width of abrupt junction is (q = 1.6×10^{-19}C. $\epsilon_s = 16$, $\epsilon_0 = 8.875 \times 10^{-12}$ F/m)
A) 6μm (B) 1μm (C) 0.6μm (D) 0.1μm

9. The ac resistance of a forward biased p-n junction diode operating at a bias voltage V and carrying current I is
(A) zero (B) a constant value independent of V & I (C) V/I (D) ΔV/ΔI

10. The deplection layer across a p^+ - n junction lies
(A) mostly in the p^+ region (B) mostly in the n region
(C) equally in both the p^+ & n region (D) entirely in the p^+ region

11. A p-n diodes dynamic conductance is directly proportional to
(A) the applied voltage (B) the temperature (C) its current (D) the thermal voltage

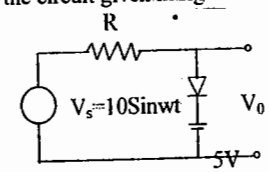
12. In the circuit shown in figure. If $e_1 = 2V$, $e_2 = 5V$, $e_3 = 1V$, & E = 2V, then which of the diodes will be conducting and what will be e_0
a) D_3; 1V
b) D_1; 2V
c) D_2; 5V
d) D_1; 5V



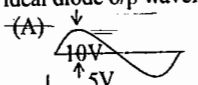
13. In a P-N junction diode space charge capacitance is proportional to V^{-n} where V is the applied bias voltage and 'n' is a constant. The value of n for step, linearly graded and diffused junctions would be respectively.
(A) 1/2, 1/3 & 1/2.5 (B) 1/3, 1/2 & 1/2.5 (C) 1/2, 1/2.5 & 1/3 (D) 1/3, 1/2.5 & 1/2

14. The current through a PN diode with V volts applied to P region relative to N region (where I_0 is the reverse saturation current of the diode, *m* the ideality factor, K boltzmann constant, T absolute temperature and q the magnitude of charge of electron) is
(A) $I_0 (e^{-qv/mkT} - 1)$ (B) $I_0 (e^{-qv/mkT})$ (C) $I_0 (1 - e^{-qv/mkT})$ (D) $I_0 (e^{qv/mkT} - 1)$

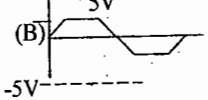
15. For the circuit given in figure assuming ideal diode o/p waveform V_0 is



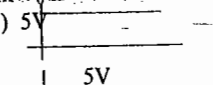
(A)



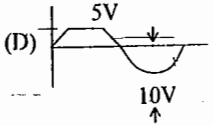
(B)



(C)



(D)



16. A silicon PN diode at a temperature of 20^0 C has a reverse saturation current of 10pA. The reverse saturation current at 40^0 C for the same bias is approximately.
A) 30 pA (B) 40 pA (C) 50 pA (D) 60 pA

17. The primary reason for the wide spread use of silicon in semiconductor device technology is
A) Abundance of silicon on the surface of the earth
(B) Large bandgap of silicon in compassion with germanium
(C) Favorable properties of silicon dioxide (SiO_2) (D) Lower meeting point

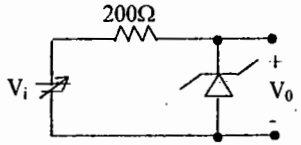
18. A silicon PN junction diode under reverse bias has depletion region of width 10μm. The relative permitivity of silicon $\epsilon r = 11.7$ and the permitivity of free space $\epsilon_0 = 8.85 \times 10^{-12}$ F/m. The depletion capacitance of diode per square meter is
A) 100μF (B) 10μF (C) 1μF (D) 20μF

19. In a P^+n junction diode under reverse bias, the magnitude of electric field is maximum at
(A) the edge of the depletion region on the P-side
(B) the edge of the depletion region on the n-side
(C) the P^+n junction
(D) the centre of the depletion region on the n-side

20. A P^+n junction has a built-in potential of 0.8 V. The depletion layer width at a reverse bias of 1.2 V is 2μm For a reverse bias of 7.2 V, the depletion layer width will be
(A) 4 μm (B) 4.9μm
(c) 8 μm
(D) 12 μm

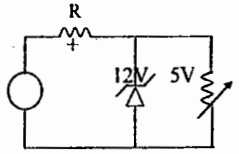
21. Which of the following is NOT associated with a P-N junction ?
(A) junction capacitance (B) charge storage capacitance
(C) depletion capacitance (D) channel length modulation

22. For the Zener diode shown in the figure , the Zener voltage at knee is 7 V, the knee current is negligible and the Zener dynamic resistance is 10Ω. If the input voltage (V_i) range is form 10 to 16 V , the output voltage (V_0) ranges from



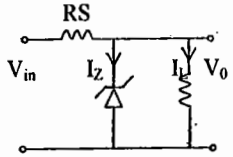
(A) 7.00 to 7.29 V
(B) 7.14 to 7.29 V
(C) 7.14 to 7.43 V
(D) 7.29 to 7.43 V

23. In the voltage regulator shown in figure. The load current can vary from 100mA to 500mA. Assuming that the Zener diode is ideal.(i.e., Zener knee current is negligibly small and Zener resistance is zero in the break down region), the value of R is
(A) 7 Ω
(B) 70 Ω
(C) 70/3 Ω
(D) 14 Ω

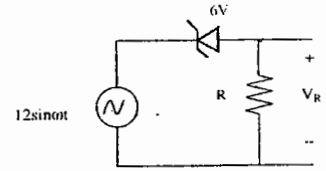


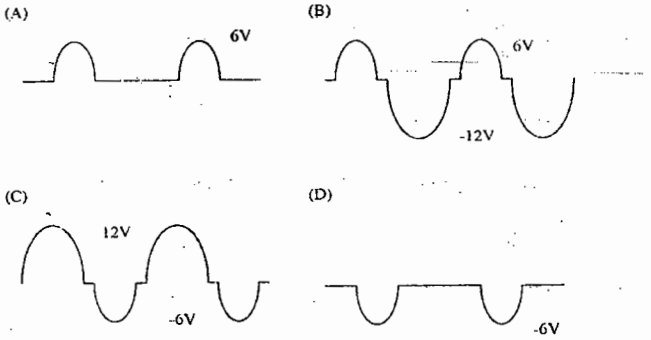
Variable load
100mA to 500mA

24. Consider the following statements regarding the circuit given in the figure, where the output voltage is constant
1) V_{in} > the voltage at which the zener breaks down
2) I_L < the difference between I and I_Z the current at which the zener breakes down
3) R_S < the zener nominal resistance.
Which of the above statements are correct
(A) 1, 2 and 3 (B) 1 and 2 (C) 2 and 3 (D) 1 and 3

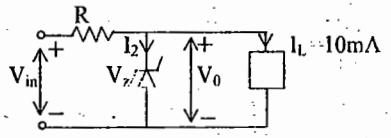


25. For the circuit shown below, assume that the zener diode is ideal with a breakdown voltage of 6 Volts. The waveform observed across R is

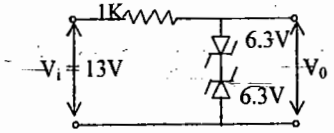




26. A zener diode regulator is to be designed to meet the specifications: I_L = 10mA, V_0 = 10V, V_{in} varies from 30V to 50V. The zener diode has V_Z = 10V, & I_{ZK}, knee current 1mA. For satisfactory operation
a) $R \le 1800\Omega$
b) $2000\Omega \le R \le 2200\Omega$
c) $3700\Omega \le R \le 4000\Omega$
d) $R > 4000\Omega$



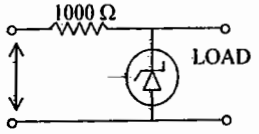
27. The o/p voltage (V_0) of the circuit shown in the figure is
a) 0
b) 5.7 V
c) 6.9 V
d) 12.6 V



28. The ideal characteristic of a stabilizer is
a) constant output voltage with low internal resistance
b) constant output current with low internal resistance
c) constant output voltage with high internal resistance
d) constant internal resistance with variable output voltage

29. The zenerdiode in the regulator circuit in Figure has a zenervoltage of 5.8 volts and a zenerknee current of 0.5 mA. The maximum load current drawn from this circuit ensuring proper functioning over the input voltage range between 20 and 30V is

(A) 23.7 mA
(B) 14.2 mA
(C) 13.7 mA
(D) 24.2 mA



30. The values of voltage (V_D) across a tunnel-diode corresponding to peak and valley currents are V_P and V_V respectively. The range of tunnel-diode voltage V_D for which the slope of its I-V_D characteristics is negative would be
(a) $V_D < 0$ (b) $0 \le V_D < V_P$ (c) $V_P \le V_D < V_V$ (d) $V_D \ge V_V$

31. Consider the following assertions
S1: For zener effect to occur, a very abrupt junction is required
S2: For Quantum tunneling to occur, a very narrow energy barrier is required
Which of the following is correct
(A) only S2 is true
(B) S1 and S2 are both true but S2 is not a reason for S1
(C) S1 and S2 and both true and S2 is a reason for S1
(D) Both S1 and S2 are false

Codes to be used for the following questions (A: Assertion, R: Reason)
(A) Both A & R are true and R is correct explanation of A
(B) Both A & R are true but R is not a correct explanation of A
(C) A is true but R is false
(D) A is false but R is true

32. **Assertion (A):** A DC voltage stabilizer is one which stabilizes the output voltage irrespective of variation in I/P voltage and load current

Reason (R): A DC voltage stabilizer uses a zener diode a cross the load to stabilize the voltage

Key:

1. c	2. b	3. d	4. a	5. b	6. a	7. b	8. c	9. d	10. b	11. c	12. c
13. a	14. d	15. d	16. b	17. b	18. b	19. c	20. a	21. d	22. a	23. d	24. b
25. b	26. a	27. c	28. a	29. c	30. c	31. b	32. b				

TOPIC 3: TRANSISTORS AND OPTO ELECTRONIC DEVICES

1. At 25°C the collector-emitter voltage drop of a silicon transistor at saturation is Approximately (A) 0.1V (B) 0.3V (C) 0.5V (D) 0.7V

2. Which one of the following is correct for the biasing of a BJT in active region

	J_E	J_C		J_E	J_C		J_E	J_C		J_E	J_C
(A)	FB	FB	(B)	FB	RB	(C)	RB	FB	(D)	RB	RB

3. For a BJT under saturation condition
(A) $I_C = \beta I_B$ (B) $I_C > \beta I_B$ (C) I_C is independent of all other parameters (D) $I_C < \beta I_B$

4. If both emitter-base and collector-base junctions of BJT are forward biased the transistor is in (A) active region (B) saturation region (C) cut-off region (D) Inverse mode

5. If $\alpha = 0.995$, $I_E = 10mA$, $I_{CO} = 0.5\ \mu A$, then I_{CEO} is
(A) 100μA (B) 25μA (C) 10.1 mA (D) 10.5 mA

6. In a BJT biased for operation at emitter current I_E and collector current I_C, the trans conductance g_m is
(A) KT / qI_E (B) qI_C / KT (C) I_C / I_E (D) I_E / I_C

7. Match List I with List II (assume List I as Region of BJT in a monolithic I(C)

List I	List II
P) Emitter	1) Moderate Resistivity
Q) Base	2) Very high Resistivity
R) Collector	3) Large size
S) Substrate	4) Very high Conductivity

(A) P-1, Q-4 R-2,S-3 (B) P-4, Q-1,R-2,S-3 (C) P-4, Q-1 R-3,S-2 (D) P-1, Q-4,R-3,S-2

8. A transistor has a current gain of 0.99 in CB mode. Its current gain in CC mode is
(A) 100 (B) 99 (C) 1.01 (D) 0.99

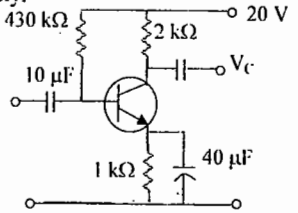
9. Match List I with List II in respect of BJT (E-B: Emitter-Base, C-B: Collector-Base, JN: Junction, FB: Forward bias, RB: Reverse Bias)

List I	List II
P) E-BJn FB & C-B Jn RB	1) Very low gain amplifier
Q) E-B & C-B Jn FB	2) Saturation condition
R) E-B Jn FB & CB Jn RB	3) High gain amplifier
S) E-B & C-B Jn RB	4) Cutoff condition

(A) P-2, Q-3 R-1,S-4 (B) P-3, Q-2,R-1,S-4
(C) P-3, Q-2 R-4,S-1 (D) P-2, Q-3,R-4,S-1

10. The circuit using a BJT with β = 50 and $V_{BE} = 0.7V$ is shown in figure the base current I_B and collector voltage V_C are respectively.

(A) 43μA and 11.4 Volts
(B) 40μA and 16 Volts
(C) 45μA and 11 Volts
(D) 50μA and 60 Volts

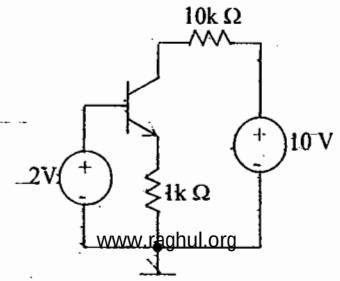


11. The phenomenon known as "Early Effect" in a bipolar transistor refers to a reduction of the effective base-width caused by
(a) electron-hole recombination at the base
(b) the reverse biasing of the base-collector junction
(c) the forward biasing of emitter-base junction
(d) the early removal of stored base charge during saturation-to-cutoff switching

12. The DC current gain (β) of a BJT is 50. Assuming that the emitter injection efficiency is 0.995, the base transport factor is
(A) 0.980 (B) 0.985 (C) 0.990 (D) 0.995

13. For the BJT circuit shown, assume that the β of the transistor is very large and $V_{BE} = 0.7$ V. The mode of operation of the BJT is

(A) cut-off
(B) saturation
(C) normal active
(D) revere active



14. For an N-channel JFET, having drain source voltage constant if the gate source voltage is increased (more negative) pinch-off would occur for
(A) high value of drain current ((B) saturation value of drain current
(C) zero drain current (D) gate current equal to drain current

15. The o/p V-I characteristics of an enhancement type MOSFET has
(A) only an ohmic region
(B) only a saturation region
(C) an ohmic region at low voltage value followed by saturation at higher voltages
(D) an ohmic region at large voltage value preceeded by saturation at low voltages

16. For a JFET in the pinch off region as the drain voltage is increased the drain current
(A) becomes zero (B) abruptly decreases (C) abruptly increases (D) remains constant

17. The threshold voltage of an n-channel enhancement mode MOSFET is 0.5V, when the device is biased at a gate voltage of 3V. pinch off would occur at a drain voltage of
(A) 1.5V (B) 2.5V (C) 3.5V (D) 4.5V

18. Match List I with List II

List I	List II
P) N-channel FET is better than p-channel	1) reverse bias increases along the channel
Q) channel is wedge shaped	2) Drain current reverse biases the channel
R) Channel is not completely closed at pinch off	3) Low leakage current at gate terminal
S) Input impedance is high	4) better performance since $\mu_n >> \mu_p$

(A) P-4, Q-1 R-2,S-3 (B) P-4, Q-2,R-1,S-3 (C) P-3, Q-1 R-2,S-4 (D) P-3, Q-2,R-1,S-4

19. In a MOS transistor, the gate source I/P impedance is
1. lower than I/P impedance of a BJT 2. Higher than I/P impedance of a BJT
3. lower than I/P impedance of a JFET 4. Higher than I/P impedance of a JFET
Which of the above statement(s) is true
(A) 1 alone (B) 2 and 3 (C) 4 alone (D) 2 and 4

20. The action of a JFET in its equivalent circuit can best be represented as
(A) current controlled current source (B) current controlled voltage source
(C) voltage controlled voltage source (D) voltage controlled current source

21. Silicon is not suitable for fabrication of LED because it is
(A) an indirect band gap semi conductor (B) a direct band gap semi conductor
(C) a wide band gap semi conductor (D) a narrow band gap semi conductor

22. The longest wave length that can be absorbed by silicon which has a band gap of 1.12 ev is 1.1 μm. If the longest wave length that can be absorbed by another material is 0.87 μm, then the band gap of that material is
(A) 1.416 ev (B) 0.886 ev (C) 0.854 ev (D) 0.706 cv

23. A particular green LED emits light of wavelength 5490°A. The energy band gap of the semi Conductor material used there is (plank's constant = 6.026×10^{-34} J sec
(A) 2.26 ev (B) 1.98 ev (C) 1.17 ev (D) 0.74 ev

24. Given that the band gap of cadmium Sulphide is 2.296 ev the maximum photon wave length for electron hole pair generation will be
(A) 5400 μm (B) 540 μm (C) 5400 A^0 (D) 540 A^0

25. Which of the following is true ?
(A) A silicon wafer heavily doped with boron is a p^+ substrate
(B) A silicon wafer lightly doped with boron is a p^+ substrate
(C) A silicon wafer heavily doped with arsenic is a p^+ substrate
(D) A silicon wafer lightly doped with arsenic is a p^+ substrate

26. Group I lists four different semiconductor devices. Match each device in Group I with its characteristic property in Group II

Group I	Group II
P. BJT	1. Population inversion
Q. MOS capacitor	2. Pinch-off voltage
R. LASER diode	3. Early effect
S. JFET	4. Flat-band voltage

(A) P-3, Q-1, R-4, S-2 (B) P-1, Q-4, R-3, S-2
(C) P-3, Q-4, R-1, S-2 (D) P-3, Q-2, R-1, S-4

27. Match List I with List II

List I	List II
P) voltage controlled device	1) BJT
Q) current controlled device	2) UJT
R) Conductivity modulation device	3) FET
S) Negative conductance device	4) IMPATT diode

(A) P-2, Q-3 R-1,S-4 (B) P-2, Q-3,R-4,S-1 (C) P-3, Q-1 R-2,S-4 (D) P-3, Q-1,R-4,S-2

28. Match List I with List II

List I	List II
P) BJT	1) Pinch off effect
Q) FET	2) Controlled rectification
R) SCR	3) Negative resistance characteristics
S) Tunnel Diode	4) Punch through effect

(A) P-1, Q-3 R-2,S-4 (B) P-1, Q-2,R-3,S-4
(C) P-4, Q-1 R-2,S-3 (D) P-1, Q-4,R-3,S-2

29. Match List I with List II

List I	List II
P) BJT	1) Voltage controlled negative resistance
Q) MOSFET	2) High current gain
R) Tunnel Diode	3) Voltage regulation
S) Zener Diode	4) High I/P impedance

(A) P-1, Q-4 R-2,S-3 (B) P-2, Q-4,R-1,S-3
(C) P-2, Q-3 R-1,S-4 (D) P-1, Q-3,R-2,S-4

30. Match items in group I with group II

Group I	Group II
P) LED	1. Heavy doping
Q) Avalanche photo diode	2. coherent radiation
R) Tunnel diode	3. Spontaneous emission
S) LASER	4. Current gain

(A) P-1, Q-2, R-4, S-3 (B) P-2, Q-3, R-1, S-4
(C) P-3, Q-4, R-1, S-2 (D) P-2, Q-1, R-4, S-3

31. Match List I with List II and select correct answer using the codes given below the lists

List - I	List - II
P. Silicon diode	1. High frequency application
Q. Germanium diode	2. Very low reverse bias saturation current
R. LED	3. Low forward bias voltage drop
S. PIN diode	4. cut off wave length

(A) P-1, Q-3, R-4, S-2 (B) P-2, Q-4, R-3, S-1
(C) P-1, Q-4, R-3, S-2 (D) P-2, Q-3, R-4, S-1

32. Match List I with List II

List I	*List II*
P. Zener Diode	1. High speed switching device
Q. Tunnel Diode	2. multivibrator circuit
R. Gum Diode	3. Voltage stabilizer
S. Pin Diode	4. Microwave Oscillator

(A) P-3, Q-1,2 R-4, S-1 (B) P-4, Q-2,4, R-4, S-1
(C) P-4, Q-1,2,4, R-1, S-3 (D) P-3, Q-1,2,4, R-4, S-1

33. Find the correct match between Group 1 and Group 2

Group I	*Group 2*
P. Varactor Diode	1. Voltage reference
Q. PIN Diode	2. High-frequency switch
R. Zener Diode	3 Tuned circuits
S. Schottky Diode	4. Current controlled attenuator

(A) P-4, Q-2, R-1, S-3 (B) P-2, Q-4, R-1, S-3
(C) P-3, Q-4, R-1, S-2 (D) P-1, Q-3, R-2, S-4

Codes to be used for the following questions

a) Both A & R are true and R is correct explanation of A
b) Both A & R are true but R is not a correct explanation of A
c) A is true but R is false ***d) A is false but R is true***

34. ***Assertion(A):*** The semiconductor devices like BJTS have a maximum temperature of operation, beyond which they do not function
Reason (R) : Extrinsic P – type and N-type semiconductors behave as intrinstic beyond that temperature and the effect of doping is lost

35. ***Assertion(A):*** The I/P impedance of insulated gate MOSFET is very high
Reason(R): The current is MOSFET's is due to majority carriers

36. ***Assertion (A):*** High power transistors are invariably made up of silicon
Reason(R) : silicon is a direct band gap semi conductor

37. ***Assertion (A) :*** A N-channel enhancement MOSFET can turn on permaturely
Reason(R): most contaminants is MOS fabrication are mobile positive charged ions and they get trapped between gate and substrate in a n-channel enhancement MOSFET, where as they are trapped on the other side of the substrate in the case of a p- channel MOSFET

Key:

1. a	2. b	3. d	4. b	5. a	6. b	7. c	8. a	9. b	10. b	11. b	12. b
13. c	14. c	15. c	16. d	17. b	18. a	19. d	20. d	21. a	22. a	23. a	24. c
25. a	26. c	27. d	28. c	29. b	30. c	31. d	32. d	33. c	34. a	35. b	36. c
37. a											

"ALL THE BEST"

OUR GATE 2009 TOPPERS

CIVIL ENGINEERING TOPPERS

S.NO	STUDENT NAME	GATE H.T NO	RANK
01	SATHISH.T	CE 1620834	1
02	NETAJI PRASAD.B	CE6920096	2
03	A.BHASKER	CE1430312	3
04	MOHD.ATAULAH KHAN	CE1430072	5
05	CH.J.P.SREE RAM	CE6690202	10

MECHANICAL ENGINEERING TOPPERS

S.NO	STUDENT NAME	GATE H.T NO	RANK
01	DESAI HARDIKKUMAR .G.	ME1500007	7
02	K.VENKATACHALAPATHI	ME1500093	9

COMPUTER SCIENCE & ENGINEERING TOPPERS

S.NO	STUDENT NAME	GATE H.T NO	RANK
01	JITHIN VACHARY	CS7580245	2
02	VENKATASATYAKIRAN.D	CS1540009	10

ELECTRICAL ENGINEERING TOPPERS

S.NO	STUDENT NAME	GATE H.T NO	RANK
01	ANIL KUMAR A.	EE6240284	2 (Test series)
02	GIRISH KUMAR DASARI	EE6760582	7 (Test series)
01	V. NARASIMHAMURTHY	EE7640633	13
02	M. NAGARAJU REDDY	EE7630195	14
03	THOKARE NITHIN.D	EE1600530	18

ELECTRONICS &COMMUNICATION ENGINEERING TOPPERS

S.NO	STUDENT NAME	GATE H.T NO	RANK
01	M.YESHWANTH	EC1440615	9
02	SANDEEP SHARATH WAIKER	EC1460408	11
03	VENKATESH SASANAPURI	EC1490210	16

INSTRUMENTATION ENGINEERING TOPPERS

S.NO	STUDENT NAME	GATE H.T NO	RANK
01	MAHESH RAVI VARMA	IN1570571	2
02	MD ABDUL RAZAK	IN1570385	3
03	MAHESHWARI RUTHIKA	IN2300299	6